



## RFID Analog Front End Design Tutorial (version 0.0)

### *Revision history*

Version	Date	Author	Contents
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## 1. Background

An RFID system (By RFID, we mean both the HF and UHF RFID) is based on a reader/interrogator and one or more tags/transponders. There are three types of RFID systems in use:

- active
- semi-active
- passive

Considering the system cost, we prefer to use the passive RFID systems as long as the performance can meet the user requirements. Nowadays, a carefully designed RFID system working in UHF frequency range can achieve the communication distance up to 4.5m at 869MHz and 500-mW ERP in anechoic chamber.<sup>i</sup> At the same time, the EPC global UHF RFID standards have finally merged into one, which paves the way to the deployment of the RFID technology.<sup>ii</sup>

As one of the key parts of the whole RFID system, the RFID tag IC is a challenge for the RFID designers. The problems like ultra low power consumption and supply voltage, big dynamic range, etc. And among all the RFID tag IC circuit blocks, the RFID front-end is something like the hardest over hardest. The front-end has to carry out all the physical level functions as well as power rectifying and regulation, clock extraction or generation, etc. However, there aren't many papers published on this issue, neither does the RFID front end. From our perspectives, we think that the more people learned on the RFID technology, the better for the deployment of it. So what we are trying to do in this paper is presenting the readers some kinds of the basic design considerations as well as circuit structures for the RFID front-end design. Nevertheless this tutorial paper cannot give the readers a ready-to-manufacturing RFID front-end blue print especially when you have to push the power consumption to the ultra low level.

The tutorial paper is divided into 3 parts. The first part is the basic structures and building blocks of a RFID front end. In the second part, we give detailed design considerations and circuits block by block. And finally we present some valuable design pitfalls or lessons in the third part. At the end, a brief summary is presented.

## 2. Overviews of RFID front-end

The major blocks and their functions of the RFID front-end are:

- **Rectifier**: to generate the power supply voltage for front-end circuits and the whole chip as well from the coupled EM field
- **Power (voltage) regulator (protector)**: to maintain the power supply at a certain level and at the same time prevent the circuit from malfunctioning or breaking under large input RF power
- **Demodulator**: to extract out the data symbols which are embedded in the carrier waveforms
- **Clock extraction or generation**: to extract the clock out of carrier (usually in HF systems) or generate the system clock by some kinds of oscillators
- **Back-scattering**: to fulfil the return link by alternating the impedance of the chip
- **Power on Reset**: to generate the chip power on reset (POR) signal
- **Voltage (current) reference**: to generate some voltage or current reference for the use of front-end and other circuit blocks, usually in the term of band-gap reference
- **Other circuits**: like the persistent node or short-term memory, ESD, etc.

Figure 1 is the block diagram of a typical RFID front-end and figure 2 is the layout of a transponder IC.<sup>iii</sup> The left middle is the RFID front-end.

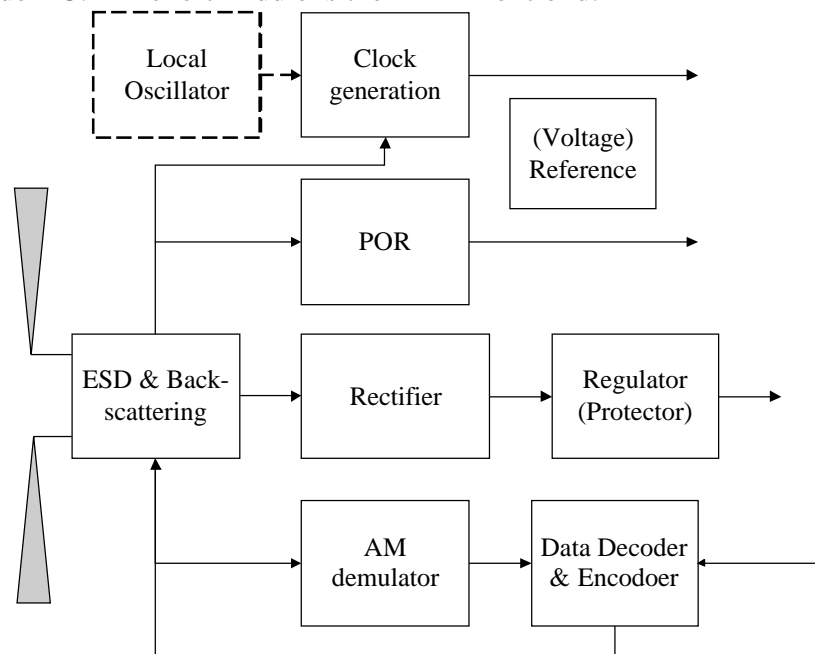


Figure 1 RFID front-end block diagram

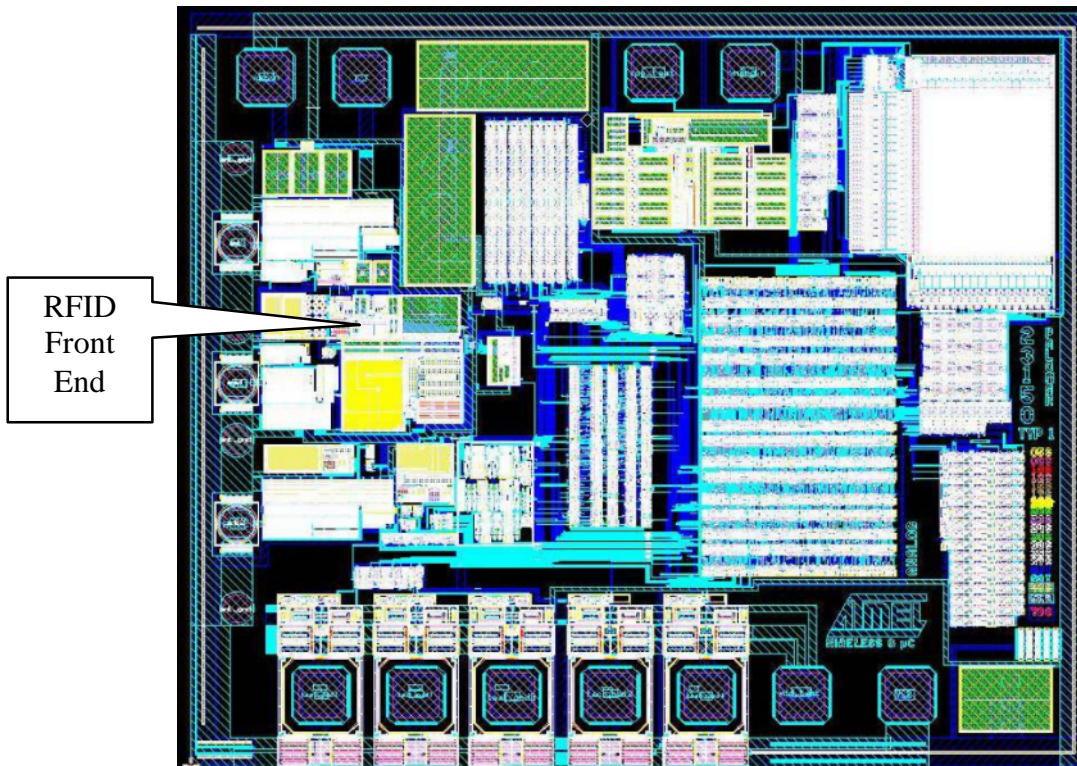


Figure 2 the layout of “Palomar demonstrator Tag IC”

### 3. Circuit blocks design

In this section, we will present detailed circuit blocks design considerations as well as the design approaches. Please note that the solutions or approaches to circuit blocks would not be limited to the ones we present and all the circuits are just for reference. Readers have to taken their own situations into considerations for their real designs.

#### 3.1 Simulation model

Before we would be able to design the circuit blocks. We have to set up a simulation model of the whole RFID system. A better simulation model is the first step to a successful design. Since the RFID front end is dealing with the EM fields, a worse simulation model will decrease the simulation fidelity and conceal some of the problems, which will cause problems in reality. In some cases, a worse simulation can even be misleading to the design. We have met some of the problems that are caused by unappropriated model and poor simulation coverage.

We can use system physics to formulate the simulation model or set up the simulation model by parameter measurement and correlation. Sometimes, we can even use real captured measurement data as the simulation input. When we find that our model deviates from the real measurement, we have to review the simulation model to find out the cause of the differences. There would be problems if we just neglected the precision of the simulation model. Like all the other modelling processes, we can always get our simulation model refined by the chip manufacture and test.

### 3.1.1 HF RFID simulation model

For the HF (13.56MHz) RFID, the systems are mainly based on magnetic coupling effects. The tags are powered by magnetic field. The magnetic field strength along an axis vertical to the coil diameter is given as:

$$H = \frac{I \cdot N \cdot r_{reader\_coil}^2}{\sqrt{(r_{reader\_coil}^2 + d^2)^3}} \quad (\text{Equation 3.1})$$

And the magnetic coupling is determined by the coupling factor  $k$ , which is given as

$$k = \frac{M}{\sqrt{L_1 \cdot L_2}} \quad (\text{Equation 3.2})$$

So we set up a simulation model by magnetic coupling. The figure 3 is the basic idea of the HF simulation model. The simulation model is based on magnetic coupling, the physical distance between reader and card is modelled by coupling factor  $k$ . Different reader and card has different antenna coil and matching network, so we have to set up different detailed simulation model for different configurations. For example, if you have to use desktop as well as the hand-held reader to access the same contact-less smart card, you have to model both of the systems to verify your design. Since there are a lot of readers available in market, it is impossible to incorporate all the readers in the simulation model(s). Usually we take several readers and tags configurations in the simulation model(s). For the HF (13.56MHz) systems, there are well-established international standards. The ISO/IEC 14443 is for the HF contact-less smart card (proximity card) and ISO/IEC 15693 is for the HF vicinity card. And the ISO/IEC 10536 is used for the HF close-coupled card and is not widely used nowadays. Besides these standards, the ISO/IEC 10373 series regulate the test method of the reader and the card. The ISO/IEC 10373-6 is for the HF proximity card compliance test and 10373-7 for vicinity card test.<sup>iv</sup> (Dealing with the HF RFID, we have to refer to ISO/IEC 18000 too.) The ISO 10373 standards present some kind of standard reader antennas with matching network. We have to at least take these antennas into our simulation model. As for the card or tag, we have to choose the coil antenna based on the proposed card or tag manufacture preferences. Like the preferred coil size and numbers, the materials to fabricate the antenna, etc. Then we can figure out the preferred coil antenna model. Normally, there are separate resonant capacitances inside the chip IC to fine-tune the resonant frequency and the quality factor of the card or tag. Anyway, we have to compromise over the preferable antenna and the card/tag performance. Besides the ISO 10373 antennas, we usually have to take some other antenna models, which are in use or we intended to use, into our modelling so as to make the design compatible with the existed system.

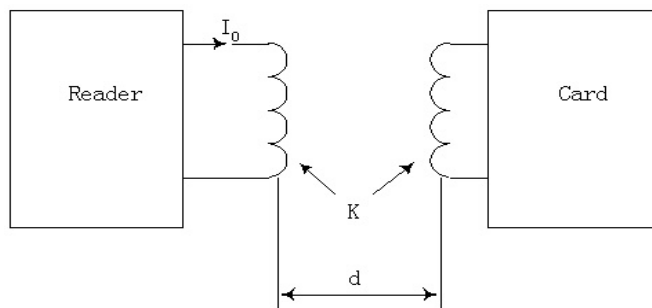


Figure 3 HF simulation model sketch

As for the coupling factor  $k$ , there are several ways to measure for a given reader and card configuration. Klaus Finkenzeller has given several approaches in his renowned “RFID handbook”. The interested reader may refer to the book for more information. The first way Finkenzeller using needs some kind of amplifier that may not be at hand. We prefer to use the way by measurement and Spice correlation. The approach is illustrated by figure 4. We can get the coupling factor  $k$  by taking the measurements and correlate the simulation results to the measurements.

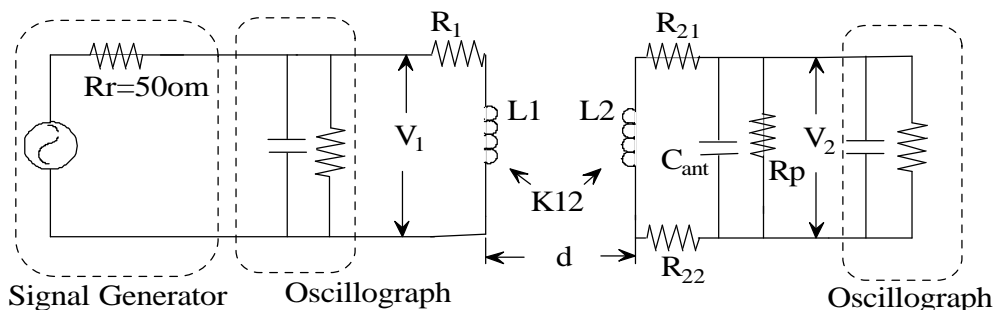


Figure 4 Coupling factor measurements

The figure 5 shows a normal simulation model to use for the HF RFID design. Besides the  $K$ , the other parameters of the simulation model can be measured directly by equipments. For example, the resistance and the inductance of the antenna. As for the simulation feed in, we will use a current source with 50ohm output resistance. The magnitude of the current source can be calculated by equation 1.1. There is a matching network between the simulation feed-in current source and the reader antenna. The figure 5 does not include chip resonant capacitance, which is usually tuned by simulation to reach maximum coupling efficiency. A specific example of the model parameters is shown in table 1. (Actually, the reader parameters was got from a special configuration of the antenna which is formed by ISO/IEC 10373 part 6. Or we can treat the reader antenna as a kind of “standard” antenna in the HF band.)

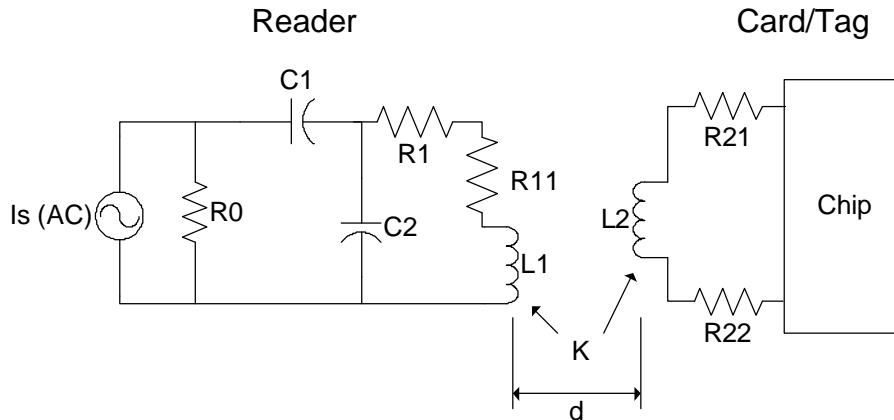


Figure 5 Proposed HF RFID simulation model

Components	Explanation	Typical value
Is	Ideal current source	13.56MHz sine waveform with DC 0 and AC effective magnitude value of 162mA
R <sub>0</sub>	Current source resistance	50 •
C <sub>1</sub>	Reader matching device	47 pf
C <sub>2</sub>	Reader matching device	184 pf
R <sub>1</sub>	Reader matching device	2 •
R <sub>11</sub>	Reader antenna resistance	0.2 •
L <sub>1</sub>	Reader antenna inductance	0.6 uH
L <sub>2</sub>	Card antenna inductance	4.08 uH
R <sub>21</sub> • R <sub>22</sub>	Card antenna resistance	$R_{21} \checkmark R_{22} \checkmark 2.64/2=1.32 \bullet$
K	Coupling factor	$d \checkmark 0\text{cm}; k \checkmark 0.12 \bullet$ $d \checkmark 15\text{cm}; k \checkmark 0.008$

Table 1 Sample parameter values for the proposed HF RFID simulation model

### 3.1.2 UHF RFID simulation model

As for the UHF RFID, we don't have much experience on the simulation model set up. Since the coupling between the reader and tags are more complicated in UHF than HF, we'd better divide the system into different parts. Basically, we divide the system into two parts. One is the reader, especially the reader antenna. And the other is the tag. Since the reader antenna can be treated as a different task for the system design, we can focus our modelling efforts on the tag side. We model the tag as a chip (with inside impedance matching circuits) and an antenna. The RF power as well as modulated signals can be modelled as a voltage source serially connected with the antenna.

For the tag antenna, we start from the simplest half wavelength dipole antenna. Although dipole and monopole antennas are not necessarily the best candidates for UWB antennas, they are easy to manufacture and low cost.<sup>v</sup> The figure 6 is the electrical equivalent of half wavelength dipole antenna presented in <sup>v</sup>. The Voltage

source  $V_{tx}$  and  $R_s$  representing the output signals. The  $R_l$  stands for the antenna loss resistance, the  $R_r$  is the radiation resistance of the antenna. The  $R_l$ , which is 1Meg ohm, is used for Spice convergence. The  $C_2$  is used to improve the performance of the antenna above resonant frequency  $f_0$ . Since the antenna is a linear network, we can use a voltage source for  $V_{rx}$  to simulate the antenna receive. And because of the fact that we are interested in are the passive UHF RFID systems, whose return-link (tag to reader) is fulfilled by alternating the tag chip impedance, we can eliminate the voltage source  $V_{tx}$  and  $R_s$  for our simulation model.

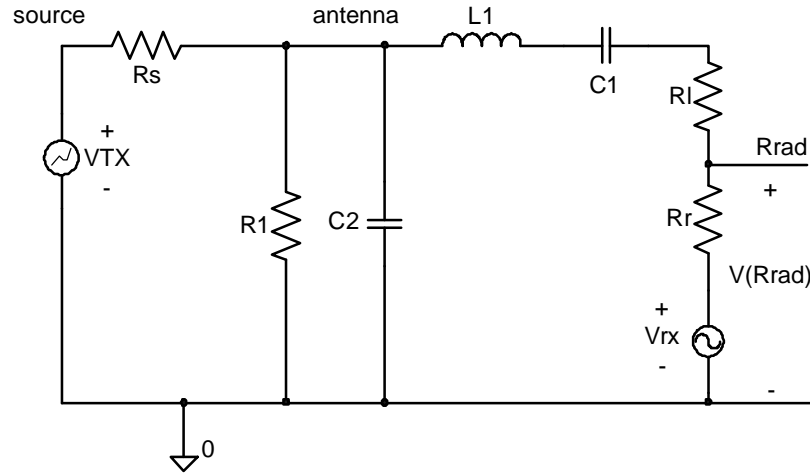


Figure 6 Electrical equivalent of a half wavelength dipole antenna connected to a 50-ohm source  
The equations for the above equivalent circuits are given as:

$$Z_a = \frac{V}{I} = (R_r + R_l) \cdot \left(1 + j\omega \frac{L}{R_r + R_l} - j \frac{1}{\omega(R_r + R_l)C}\right) \quad (\text{Equation 3.3})$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi \sqrt{LC}} \quad (\text{Equation 3.4})$$

$$Q = \frac{\omega_0 L}{R_r + R_l} = \frac{1}{R_r + R_l} \sqrt{\frac{L}{C}} \quad (\text{Equation 3.5})$$

In our RFID rectifier structures analysis, we have already used this kind of antenna model for simulation.<sup>vi</sup> We re-modeled the  $L_1$  and  $C_1$  to move the resonant frequency from 1.25GHz in <sup>v</sup> to 900MHz. At the same time, we don't include the loss resistance and  $C_2$  at this time. The parameters of the antenna model are (assume the  $Q=5$ ):

$$L_1 = 64.55 \text{ nH}$$

$$C_1 = 484.5 \text{ fF}$$

$$R_r = 73 \text{ ohm}$$

$$R_l = 0 \text{ ohm}$$

With the antenna gain about 0dB and 500-mW ERP, the input power at the distance 2m (in anechoic chamber) is about 150-uW. We can calculate out the  $V_{rx}$  (peak-to-peak) value of model by short-connect the node 'antenna' in figure 6 to ground.

$$V_{rx(p-p)} = 2\sqrt{2} \cdot \sqrt{P \cdot R_r} = 2\sqrt{2} \cdot \sqrt{150 \mu\text{W} \cdot 73} = 0.296 \text{ V}$$



Besides the power transfer, the EM fields are used to carry the signals as well. We have to take the modulated signals into our simulation as well. Any RF device in use has to be compliant with local EM regulations. The RFID reader also has to be compliant with the regulations. The interested readers may find RFID related regulations in these references.<sup>vii</sup> The European regulation over UHF RFID is stricter than the FCC regulation, so we base our simulation model on the European regulations.

The reader has to pass its base band signals through filters to make the signal spectrums under the regulation spectrum masks. We usually use a raised wave cosine filter as the base band signal filter. The design of the filters is usually carried as another work within the whole RFID system. We will presume that we already have the filters, which makes the signal spectrum compliant with the regulations. Then what we are going to do is to choose a typical command from the command set and generate a base band data sequence. Then encode the data sequence to specific channel encoding scheme (for instance, Pulse Interval Modulation). Then we pass the encoded sequence through the filters and grab the output time domain response sequence as the data vectors for the simulation model.

Since we may have different channel encoding methods, different data rates and different commands, it is better to make some kind of the automatic generation software or script to do the work. We use the MATLAB to fulfil the reader filters as well as the sequence generating. In annex A, we present the sample MATLAB script for the filter and data envelop generation. After the data envelope is generated, we use a small function to output the data envelop sample points with timing to a text file. Then we may be able to read the text file in as a PWL control voltage for the voltage controlled voltage source in the spice simulation file as the antenna excitation. You may find the details of the MATLAB function and the spice simulation file in Annex B.

The figure 7 is the base band signal envelop before and after a raised cosine filter. The figure 8 is the spice excitation plot. Since all the work is carried out automatically, it is easy to change the encoding method and other parameters. And the waveform enveloped not only affected by the channel encoding, filter parameters, it is also affected by the modulation method. We use simple AM modulation to get the waveforms like figure8. If you choose other modulation approaches, the waveform envelopes would be different from what we show in our example. The better the simulation coverage, the more configurations we have to take into our simulation model. Fortunately, the computer can do most of the work after you set up the simulation environment.

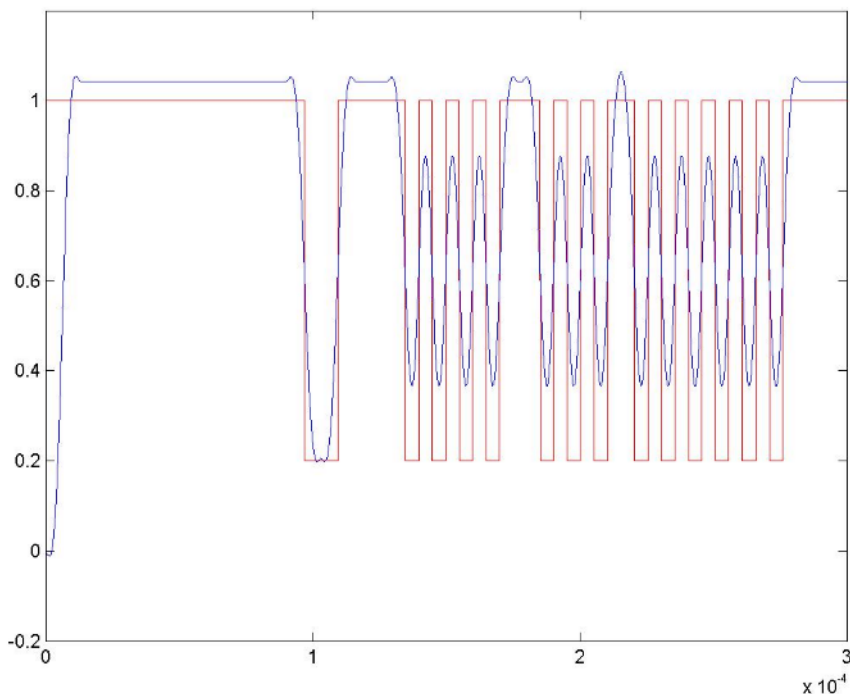


Figure 7 base-band signal envelop before and after a raised cosine filter by MATLAB 6.1

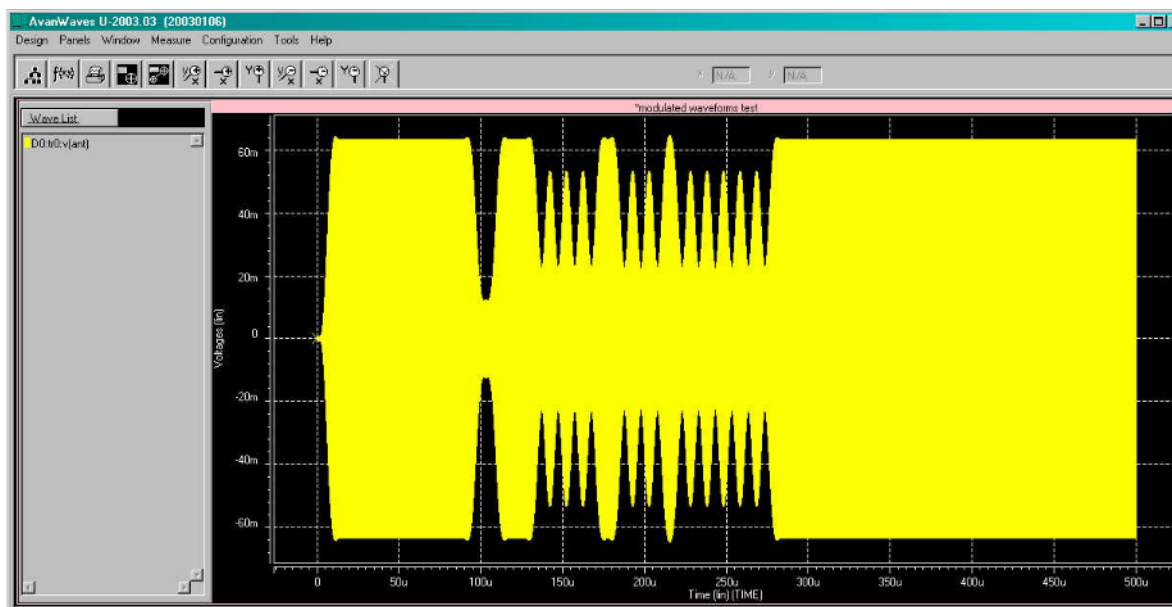


Figure 8 50ohm load voltage waveforms (half wave length dipole antenna and 150uW 900MHz RF input power, no resonant circuits) by Hspice and Avanwaves 2003

### 3.2 Rectifier

Rectifier is used to generate the needed supply power for the whole chip and be treated as one of the key parts of the RFID front-end. We have done analysis and comparison over different rectifier structures in our former research work. The readers may find more information on rectifier structure in the papers <sup>vi</sup> and <sup>viii</sup>.

After comprehensive analysis and comparison, we have found that no single structure can achieve over-all better performance for different loads and/or input voltage levels. And we found that NMOS and PMOS gate cross-connected bridge rectifier can achieve over-all good PCE performance at smaller input voltage level (around 2V for CSM06 CMOS process). While at higher output voltage level, PMOS diode-connected bridge rectifier has better performance. And without the technology integration limitation, the diode (with low turn-on voltage and fast switch speed, i.e. Schottky diode) voltage multiplier structure can achieve the best performance under the minimum input voltage level.

Since the efficiency of the rectifier is most critical at minimum RF input power, we may choose the rectifier structure according to the performance at minimum RF input power. The table 2 lists the best choice according to the requirements and constrains at minimum RF input power. You may see that you would be able to use some of the structures by sacrificing the output power, which means you have to decrease the overall chip power consumption. Otherwise, you would not be able to power up the chip.

Minimum Input Voltage (V <sub>p-p</sub> )	Preferred Output DC Voltage	Possibility of special device (constrain 1)	Available output power (constrain 2)	Choice
Around 1 V <sub>th</sub>	> 3 V <sub>th</sub>	Yes	High	Diode voltage multiplier (charge pump)
> 2 V <sub>th</sub>	~= or < 2V <sub>th</sub>	Yes	High	Diode voltage multiplier with less stages
>2 V <sub>th</sub>	~= or < 2V <sub>th</sub>	No	Middle	NMOS PMOS gate cross-connected bridge rectifier
> 4V <sub>th</sub>	> 3V <sub>th</sub>	No	Small	PMOS diode-connected bridge rectifier

*Table 2 Possible rectifier structure choice based on requirements and constrains*

Note: V<sub>th</sub> standards for MOS transistor threshold voltage and the available output power is according to fixed input power.

### 3.3 Regulator (Protector)

The regulator (protector) has two major functions. One is to regulate the front-end output supply voltage level to a preferred value and within a preferred range. For example, output voltage to the digital core is 2.5V. The other is to protect the inner circuits from breaking at high RF input power. As we know, The EM field strength may vary in the magnitude of tens even hundreds of times at different physical locations. If all the conditions remain the same, the RF input power to the tag chip

can vary in the same magnitude of the EM field strength. There must be circuits inside the analogue front end to overcome the variation.

Because of the fact that the EM field variation is huge, a single circuit block cannot handle the situation. We usually use different sub circuit blocks to carrier the protection and regulation functions separately. Nevertheless, the circuit structures are similar. There are two basic approaches to fulfil the regulation/protection. One is the shunt regulation and the other is coupling factor attenuation.

As we know, for a fixed input electric power, the higher the current, the lower the voltage. So what the shunt regulator does is to bypass the surplus power to some shunt routes so as to keep the output voltage unchanged. Although there might be a lot of implementations of the shunt regulation circuits, the basic ideas of the shunt regulation are the same. The shunt regulator is a kind of negative feedback system. The value we have to control is voltage, so we have to use some voltage reference as the control input. And the voltage difference between the reference and the input (or ratio of the input) is fed into or magnified then fed into some kind of voltage controlled variable resistors so as to change the overall output current and suppress the output voltage variations.

The figure 9 shows a kind of simple solution. It uses ratio of the output voltage to control the  $V_{gs}$  of a MOS transistor, which is M3, working in the saturation region. This MOS transistor serves as the variable load. By varying the current of the MOS transistor M3, the overall load current of the rectifier output will be changed.

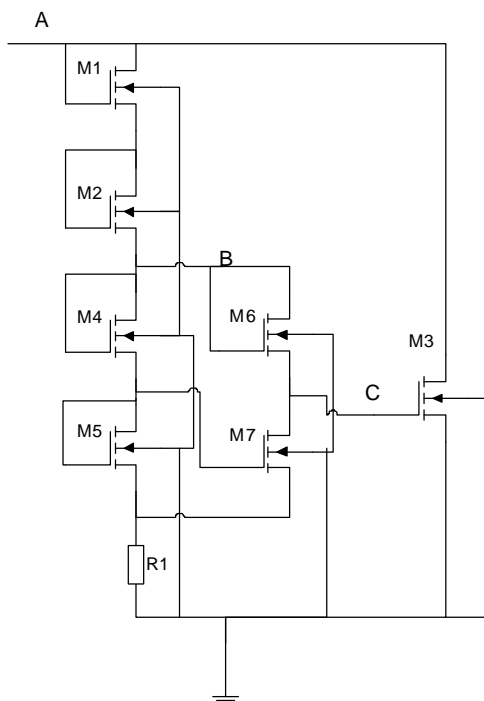


Fig. 9 A simple approach of the shunt regulator (protector)

The transistor M5 size is much larger than the one of M7, thus most of the current will pass through the branch of M4 and M5 rather than M6 and M7. With same size, gate voltage and drain voltage, the drain source voltage drop of M6 is smaller than M4.

Thus the M7 is also working in the saturation region. And the voltage of node C follows voltage of node B by a  $V_{th}$ . Without considering the substrate bias, the transistor M3 can be turned on after the voltage of node A raises above  $4V_{th}$ . If we consider the substrate bias, the turn on voltage will be even higher, like  $5V_{th}$  or more.

In order to find out the way to set the transistor parameters for the simple shunt regulator, we have to take some analysis. In order to simplify the calculation, we omit the second-order effects, like the substrate bias, channel length modulation, etc. At the same time, we still hold the assumptions made in last paragraph. So we can get:

$$V(C) = V(A) - V_{gs1} - V_{gs2} - V_{gs6} = V(A) - 3V_{gs1}$$

$$V(D) = V(A) - V_{gs1} - V_{gs2} - V_{gs4} - V_{gs5} \approx V(A) - 4V_{gs1} \quad (\text{Equation 3.6})$$

$$V(D) = I(M_1) * R_1 \quad (\text{Equation 3.7})$$

$$I(M_1) = \frac{1}{2} b_{M1} (V_{gs1} - V_{th})^2 \quad (\text{Equation 3.8})$$

By 3.6, 3.7 and 3.8, we can get the  $V_{gs1}$ , which is given by:

$$V_{gs1} = V_{th} - \frac{2}{k} + \frac{1}{k} \sqrt{k[V(A) - 4V_{th}] + 4}, \quad (k = \frac{1}{2} b_{M1} \cdot R_1) \quad (\text{Equation 3.9})$$

By equation 3.9 we can derive:

$$\frac{\partial V_{gs1}}{\partial V(A)} = \frac{1}{2\sqrt{k[V(A) - 4V_{th}] + 4}} \quad (\text{Equation 3.10})$$

We can find that the existence of the resistor  $R_1$  serves as an attenuator besides the function of limit current flow over the reference branch from equation 3.10. Without the  $R_1$  ( $R_1 = 0$ ),  $V_{gs1}$  will be  $\frac{1}{4}$  of the voltage of node A if we omit the substrate bias effect and voltage of node C will follow the voltage of node A at the rate of  $\frac{1}{4}$ . The  $R_1$  will attenuate the  $V_{gs1}$  variation caused by  $V(A)$ . With the attenuation, the node C can follow up the voltage of node A at a higher rate. If we assume that the  $k$  approaches infinity, we can push the equation 3.10 to another limit. We can see that the  $V_{gs1}$  will remain constant as  $V_{th}$  and the voltage of node C will directly follow the voltage of node A. So, actually, the attenuation of  $V_{gs1}$  is actually a kind of gain from the whole circuit block perspective.

By equation 3.9, we can get the current of transistor M3, which is given by:

$$I(M_3) = \frac{1}{2} b_{M3} [V(A) - 4V_{th} - \frac{3}{k} \sqrt{k[V(A) - 4V_{th}] + 4} + \frac{6}{k}]^2 \quad (\text{Equation 3.11})$$

Substitution with two limits of  $k$ , we can get:

$$I(M_3) = \frac{1}{2} b_{M3} [\frac{1}{4} V(A) - V_{th}]^2, \quad R_1 = 0 \quad (\text{Equation 3.12})$$



$$I(M_3) = \frac{1}{2} b_{M3} [V(A) - 4V_{th}]^2, \quad k = \frac{1}{2} b_{M1} \cdot R_1 = \infty \quad (\text{Equation 3.13})$$

After the above analysis, we can choose the transistor parameters according to the system specification. We start from the input RF power dynamic range. The RF power dynamic range is usually given by the regulation and the chip power consumption estimation. The minimum chip power consumption is the index of the maximum operation distance that the tag can work at. And the regulation forms maximum RF input power.

For the HF case, we can convert the maximum magnetic field to the form of maximum input power. For the UHF case, with the maximum ERP about 500mW and antenna gains of 0dB, we can estimate the maximum input power to the tag is around 60mW for a distance of 10 cm. The dynamic range of the UHF range input power is around 100mW or so.

The next step is to determine the maximum tolerant output voltage, which is determined by the stack numbers of the NMOS transistor in figure 9. You can decrease the stack number to get a low turn-on voltage, however, you have to recalculate the current functions anyway. For the configuration of figure 9 and taking in the substrate bias effects, the turn-on voltage of the shunt regulator is around 6 volts. By substituting the M1 and M2 with PMOS counterparts, you can suppress the substrate bias effects a little bit so as to decrease the turn-on voltage.

After you decide the turn-on voltage of the shunt regulator and get the functions. You may decide the regulator output voltage variations that you can withstand. Like 1 volt or 0.5 volts. Then by equation 3.12 and 3.13, we can get the  $b_{M3}$  range and so as the  $k$ . For example, for the output voltage variation of 1 volt and the input power range about 100mW, we can get that the needed  $b_{M3}$  to be 0.2 to 3.2. Normally, we can get  $b$  of around 1m for a W/L ratio 10 NMOS transistor (assume that the  $m_n \cdot C_{ox} = 100\mu$ ), which means we should use a transistor whose W/L ratio is 1000 to get a  $b$  around 1. So we have to balance the size of M3 and the value of  $k$ . If we choose the W/L ratio of M3 to be 500 and get the  $b_{M3} = 0.5$ , the value of  $k$  would be around 34. A  $k$  of 34 can be achieved by  $b_{M1} = 1m$  and  $R_1 = 68K$ . In really implementation, we can substitute the resistor R1 with a transistor working in the triode region. The above example is not the single solution of the real implementation of the shunt regulator structure of figure 9. Usually, we have to make the first order calculation by hand like what we did previously firstly, and then use the circuit simulation tool to fine-tune the circuits.

Since the maximum voltage gain of the voltage of node C over regulator input voltage is only 1 for the simple structure. So if we want to suppress the voltage variation to be even much smaller or accommodate a larger input dynamic range, we have to use a fairly large shunt transistor. What we usually do is to use an amplifier to increase the

gain of the shunt transistor control voltage (the first stage). Figure 10 is a kind of shunt regulator structure with amplifier stage between the sample/compare and the shunt transistor.

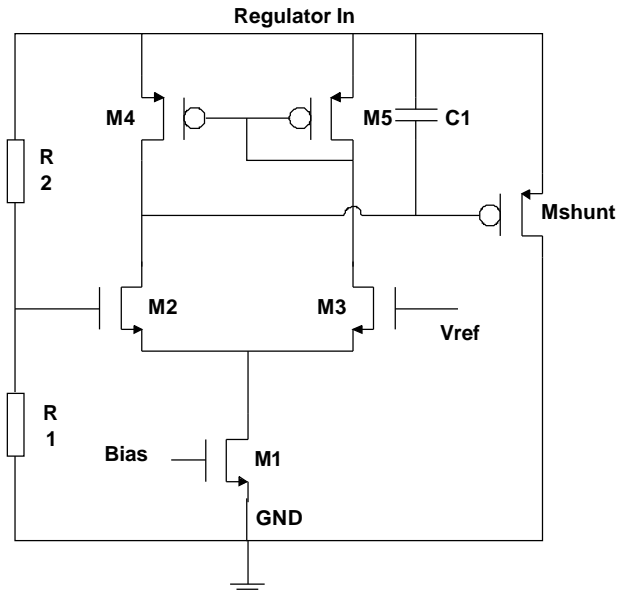


Fig. 10 An approach of the shunt regulator (protector) using amplifier

The parameters calculation or analysis process is the same as the simple structure. The difference is the case of the structure with amplifier, you can divide the overall gain to two parts, one is the gain of shunt transistor, which is the same as simple approach, and the other is the gain of the comparator. Although we may increase the gain of the amplifier so as to decrease the gain of the shunt transistor, we still have to some kind of the limitations. Firstly, the output range of the amplifier is fixed for a fixed supply range. So with that amount of output range, the output current variation is fixed for a certain  $b_{Mshunt}$ . Secondly, there are current limitations over MOS transistors. A transistor with a certain W/L ratio can over work under a certain current limitation safely. Normally, every W/L can withstand 1mA. So we cannot decrease the shunt regulator size dramatically. The purpose of adding the amplifier is mainly for better output voltage suppression. Another advantage of the structure with amplifier is that the turn-on voltage can be controlled precisely. We can use some kind of high precision voltage reference like band-gap reference as the turn-on threshold.

Another issue we have to take into account for the amplifier solution is the stability. The original simple structure is a single order system, so inherently stable. By adding the amplifier, we have to make sure the system would not suffer stability problems.

Besides the physical location change, there are other causes of the tag input RF power variation. One is caused by modulation. As we know, the downlink signalling or the signalling from reader to tags is carried by some kind of modulation over the carrier. Back scattering causes the other. As we know, the uplink signalling or the signalling from tags to reader is carried by tag input impedance modulation. So the input RF power would be changed during the communication between the reader and tag. The



RF power variation caused by these two causes is usually faster than the physical location change, which is caused by the moving of tag. So the shunt regulator has to handle these two causes of variation, too. Unlike the physical location change, we don't want to suppress the voltage envelop change, so what we have to do is control the bandwidth of the shunt regulator to be much smaller than the signalling bandwidth. Otherwise there would be suppression over the carrier modulation and make the demodulator hard to decode. So we have to control the close loop bandwidth of the shunt regulator as well during the design.

We can use the above structures as the input protector or voltage regulator without many modifications. However, in order to get a well-rounded regulator design, we have to consider another issue: the power consumption variation of the chip (digital core). For contact-less smart card, there is a challenge to isolate between the receiver and the noisy digital circuitry<sup>ix</sup>. Since the received power is only dependent on card or tag location at a certain time, and as we know the shunt regulator bandwidth could not be set high in order to prevent the attenuation of modulated signals, any change in current results directly in a change in voltage. Since the power signal and the received data signal are the same, the impulse currents generated by the digital circuits may greatly impact the quality of the received signal. The chip power interference also exists in the UHF RFID tags. The chip power interference will not only affect the chip receiver, but also affect the reader receiver. Since the reader has to pick up the weak back-scattering signals, receiver sensitivity is so high and can easily pick up the broadcasted power consumption variations of close tags. The interference will degrade the system signal noise ratio.

Besides the interference to the receivers, the power consumption variation is also a kind of security threat. A strong means of key attack is power analysis. Simple power analysis involves looking at the current signature of a device to determine what is going on inside a device. Differential power analysis uses two simple power analyses with a difference in only a single bit to identify exact functions at a precise time within a device. Differential power analysis is a large security threat<sup>x</sup>. And like what we said before the power variation is broadcasted in air and makes the power analysis attach more easily. So we would better to incorporate some kind of isolation circuits in the regulator to isolate the digital core power supply from the outside. The paper<sup>ix</sup> has presented a kind of isolation approach as showed in figure 11. The regulator with isolation in figure 11 contains two major parts. The right portion is the same as the shunt regulator we described early. The difference is this regulator has a much larger bandwidth than the former one. It has to suppress the voltage variation caused by digital core power consumption variations. The left portion is actually a controlled current source. Once the input power voltage reaches above a certain level, most of the current of M1 will pass through M4 and mirrored to Mreg to supply the digital core. And the current of M1 is mirrored from some precise reference. Since the excess current will be shunt by the regulator after the current source. Once the Mreg is turned on, the output current is fixed and will not varied with the core power consumption. So the output current of Mreg has to be tuned to meet the maximum current consumption of the core.





frequency. If we change the tag input capacitance, we would change the resonant frequency so as to the coupling factor. With less coupling factor, the power transferred to the card/tag would be decreased. The implementation is not far different from the shunt regulator. Both of the approaches use the some kind of reference and comparator; the difference is the control part. The former approach controls a kind of voltage-controlled resistor, the latter one controls a kind of voltage controlled capacitor or varactor. The analysis is also the same as the former approach. We have to determine the varactor change magnitude by analysis over the relationship between capacitor value and resonant frequency so as the coupling factor. Then we might be able to find the suitable varactor value and the corresponding input control.

In the UHF system, the reader and tag can be modelled as a kind of back-scattering system. The maximum power transfer happens when the chip impedance is fully matched with the tag antenna. Without match, part or even whole of the input RF power will be reflected back. So we might use varactor to control the chip input impedance. Once the input RF power exceeds a certain level, we might change the varactor controlled voltage to get different input impedance so as to make part of the RF power reflected back to air. When we use this kind of approach, we have to be very careful on the control bandwidth. Since the backward signalling is also carried by back scattering, we have to make the protection control frequency far away from the back-scattering signalling frequency, which is usually around several hundred kilo hertz.

We will not describe the details of the varactor implementation. We will cover this part in the section of back modulator.

### 3.4 Demodulator

Demodulator is another key circuit block inside the analogue front end. Although the modulation schemes to use in the reader might be different, some of them are amplitude modulation, and some of them are phase modulation. The analogue front-end demodulator can demodulate is only in the form of amplitude change or “dip”. So the demodulator is actually an edge detector.

The figure 12 presents a basic structure of demodulator. After the input carrier waveform is passed through a rectifier and envelop detector to extract the envelop out. The low-pass filter after the envelope detector use to filter out the carrier ripple noise residue. Then the signal and its low pass filtered one is fed into a hysteresis comparator to generate the output.

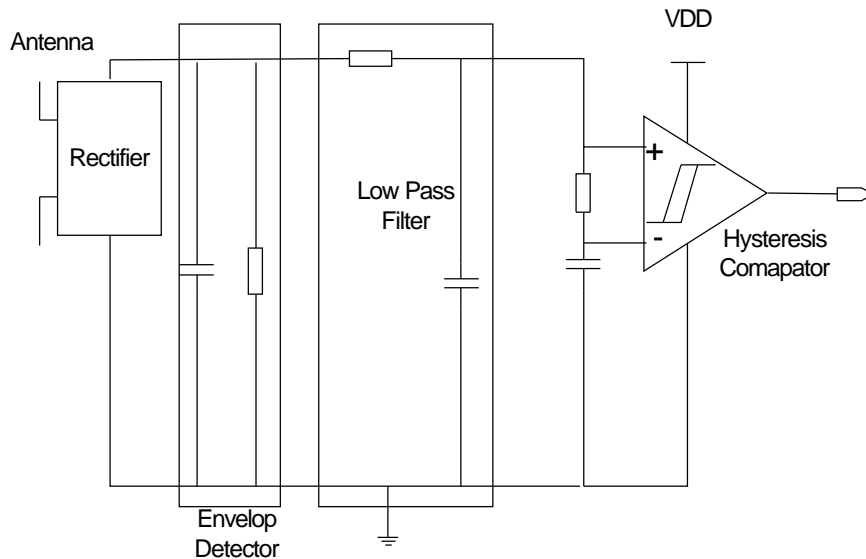


Fig. 12 Basic Structure of Demodulator

The envelope detector is the simple and cheap form of AM demodulator. One problem comes along with the simple envelope detector is the non-linearity of the rectifier. And this will cause the output distortion. However, the RFID system only transfers two logic value binary codes through the air. So the distortion of the envelope detector is not a critical problem. The other problem is the *ripple* and the *negative peak clipping*. The following contents are extracted from the resource <sup>xi</sup>. The readers are encouraged to browse this resource, not only on that specific part of AM modulation and demodulation, but also other parts. And the analysis is based on single diode envelope detector. If we use full wave rectifier, the ripple would be decreased to half of the analysis.

Consider what happens when we have a carrier frequency,  $f_c$ , and use an envelope detector whose *time constant*,  $t = R \cdot C$ . The time between successive peaks of the carrier will be  $T = \frac{1}{f_c}$ . Between each carrier peak and the next the capacitor voltage will therefore be discharged to

$$V'_{peak} = V_{peak} \text{Exp}\{-T/t\} \quad (\text{Equation 3.14})$$

Provided that  $T \ll t$ , the peak-to-peak size of the ripple will therefore be:

$$\Delta V \approx \frac{V_{peak} T}{t} = \frac{V_{peak}}{f_c t} \quad (\text{Equation 3.15})$$

A sudden, large reduction in the amplitude of the input AM wave means that capacitor charge isn't being 'topped up' by each carrier cycle peak. The capacitor voltage therefore falls exponentially until it reaches the new, smaller, peak value. To assess this effect, consider what happens when the AM wave's amplitude suddenly



reduces from  $V_{peak}$  to a much smaller value. The capacitor voltage then declines according to

$$V_{drop} = V_{peak} \text{Exp}\{-t/t\} \quad (\text{Equation 3.16})$$

This produces the negative peak clipping effect where any swift reductions in the AM wave's amplitude are 'rounded off' and the output is distorted. Here we've chosen the worst possible case of square wave modulation. In practice the modulating signal is normally restricted to a specific frequency range. This limits the maximum rate of fall of the AM wave's amplitude.

We can therefore hope to avoid negative peak clipping by arranging that the detector's time constant  $t \ll t_m$  where  $t_m = 1/f_m$  and  $f_m$  is the highest modulation frequency used in a given situation.

The above implies that we can avoid negative peak clipping by choosing a small value of envelope detector time constant. However, from equation 3.15 we can see that in order to minimise ripple we want to make the time as large as possible. In practice we should therefore choose a value which is given by 3.17 to balance between *ripple* and the *negative peak clipping*.

$$1/f_c \ll t \ll 1/f_m \quad (\text{Equation 3.17})$$

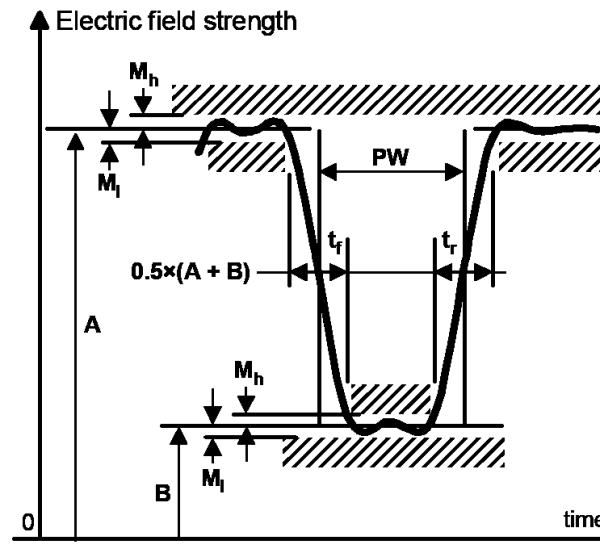
This is clearly only possible if the modulation frequency  $f_m \ll f_c$ . Envelope detectors only work satisfactorily when we ensure this inequality is true.

For example, the maximum forward link data rate in the UHF EPC class-1 generation 2 is 120K. And it satisfies the frequency constrains for the envelope detector. We may choose the time constant to be around 0.1us to 0.5us.

The design of the edge detection has several considerations. One is the low pass filter's parameter, another is the hysteresis level of the comparator, and the third one is the comparator sensitivity.

The low pass filter parameter is determined by the reader to tag data rate, the coding and the envelope mask. Since the comparator will compare the signal itself and its low-pass filtered one. The filter bandwidth should be smaller than the signal bandwidth at least. Otherwise, there would be no difference for the two input signals to the comparator. There are normally some parts in the RFID air interface protocol to describe the data envelope. Figure 13 and table 3 give an example of the data envelope regulation.

## ASK Modulation



*Fig. 13 ASK modulation waveforms envelope sample*

Data Rate	Parameter	Symbol	Min	Typical	Max	Units
40Kbps	Modulation Depth	(A-B)/A	80	90	100	%
	RF envelope ripple	Mh=Ml	0		0.05(A-B)	
	RF envelope rise time	$T_{r,10\%-90\%}$	0		0.33PW	ms
	RF envelope fall time	$T_{f,90\%-10\%}$	0		0.33PW	ms
	RF envelope pulse width	PW	6.6		13.1	ms

*Table 3 RF envelope parameters of figure 13*

Note: the data coding is Modified Miller

From the tag's perspective, the smaller bandwidth signals are difficult for the demodulator, while the smaller bandwidth is better for the reader to meet the EM regulations. So the design of the demodulator normally starts with the smallest bandwidth input signals. Let's use the parameters in the table 3 as an analysis example. The data rate is 40kbps, which means the period of data is 25us. The maximum rising and falling time is about 4us according to the table 3. If we treat the rising and falling edge as cosine wave shape, the frequency of the cosine wave is 125KHz. We choose this frequency as the cut-off frequency of the R-C form low pass filter. By the RC low-pass filter cut-off frequency equation:

$$f_{cut-off} = \frac{1}{2\pi RC} \quad (Equation 3.18)$$

We would be able to get the value of R and C. For the cut-off frequency of 125KHz, the R\*C or the time-constant is 1.27us. We can choose the R equals 130k ohm and the C value to be 10pf. As we know, the values of R and C may have a lot of combinations. The ways we choose usually have to consider the implementation. There are several constrains over the upper limit of the capacitor. Firstly, for a specific time-constant, the larger the capacitor, the smaller the resistor and this means



larger power consumption for the R-C filter for a given input voltage source. Secondly, the capacitor is connected between comparator input port and ground, the larger the capacitance, the smaller the AC resistance, which means worse high frequency substrate noise coupling. Thirdly, the capacitor usually takes a lot of chip area. So the capacitor cannot be very large. On the other hand, the resistors with large sheet resistance values usually have large process variations, and the thermal noise is proportional to the resistance value. So the choice of capacitance should be a kind of check and balance. The value we gave previously is a kind of balance. As an alternative to the passive RC low-pass filter, we might also use the active low-pass filter to generate the input signals to the comparator. When we use the active low-pass filter, we have to budget the overhead power consumption so as to meet the overall power consumption constrains.

Finished the first two parts of the demodulator, we come to the comparator. The comparator is a mature building circuit block and widely used in analogue and mixed signal ICs. The comparator to meet the specification of the RFID demodulator is not difficult to design. We might start from the dynamic range. As we know, the input voltage level will be around several hundreds millivolts to several volts at different physical locations. The signal after the envelope detector and the low-pass filter should be in the same magnitude. When we have the signalling protocol and the design of envelop detector and filters, we may draw out the specification of the comparator. For example, the common mode input level to the comparator is from 100mV to 5V and the differential mode input level is about 80% of the common mode level.

Besides the dynamic range, the hysteresis level is another important parameter of the comparator. When the analogue input signals are moving slowly or contain noise, the comparator outputs may oscillate at the input near the threshold point. Besides adding the power supply bypass circuits and better isolated the comparator from the other noisy circuits, hysteresis maybe added to further resist the oscillation during output transitions. As we know, the high the hysteresis level, the better rejection of input noise and transition oscillations. However, the higher hysteresis level also means worse sensitivity and slow transition speed. So we'd better to set the hysteresis level "just" at what we need. It is harder to implement than we say "just". We might start from the minimum input level and the timing of the signal and its low-pass filtered counterpart. The minimum input differential level is determined when the envelope detector and filters are determined for a certain signalling protocol. So does the timing issue. With the level and the timing, we can draw out the specification of the hysteresis level. Like the low-pass filter cut-off frequency choice discussed previously, we have to start the analysis from the worse situation when we analysing the hysteresis level. At fast data rate, with the fixed low-pass filter cut-off frequency, the low-pass filtered signal may not reach its final value as its counter-part, like shown in figure 14. So we have to take this into consideration. In real design, we have to taken the process variations into consideration. Usually, we have to sacrifice the hysteresis level at normal case to meet the process variations.

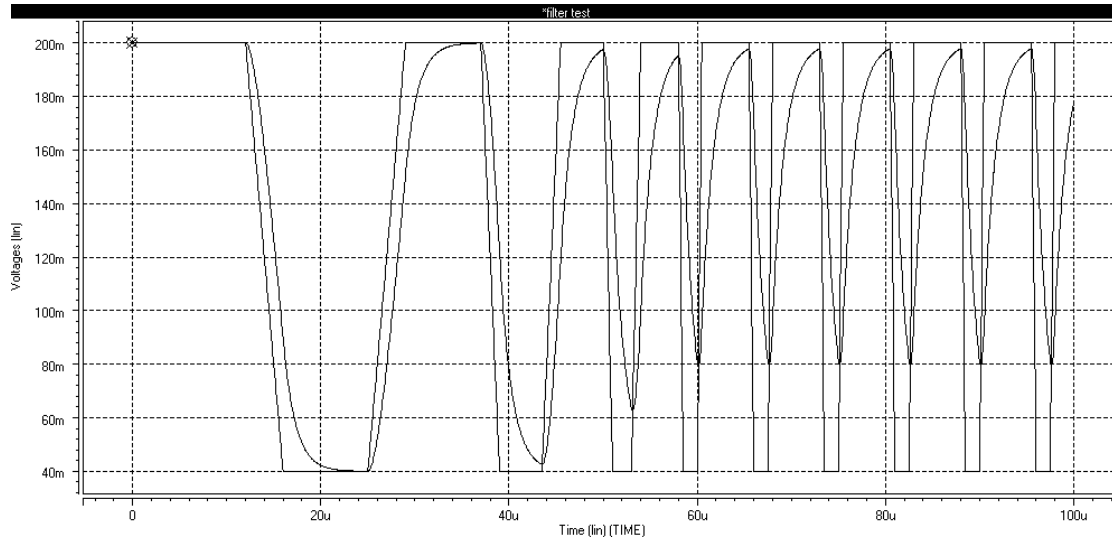


Fig. 14 fixed cut-off frequency RC low-pass filter transient analysis over different data rate

We assume that the comparator design references are available to the readers and will not go through the details of the comparator design in this tutorial.

Besides the differential comparator, we might also be able to use single transistor amplifier as demodulator. The figure 15 is a single transistor amplifier demodulator. The data envelope detector and the low-pass filter for the carrier residue filtering are probably the same as the differential approach. The signal after the envelope detector and filter is AC coupled to a single transistor amplifier to decode the data. The Mp1 and Mn1 provide the bias for the single transistor Mn2 amplifier. The amplifier uses the MP2 as the output load. The Mp3 and Mn3 are connected as inverter for the second stage. A buffer is also incorporated between the amplifier and the output. This approach has the advantage of simplicity. Simplicity usually means better chip area and power consumption. The problems related to this kind of structure are noise and worse sensitivity.

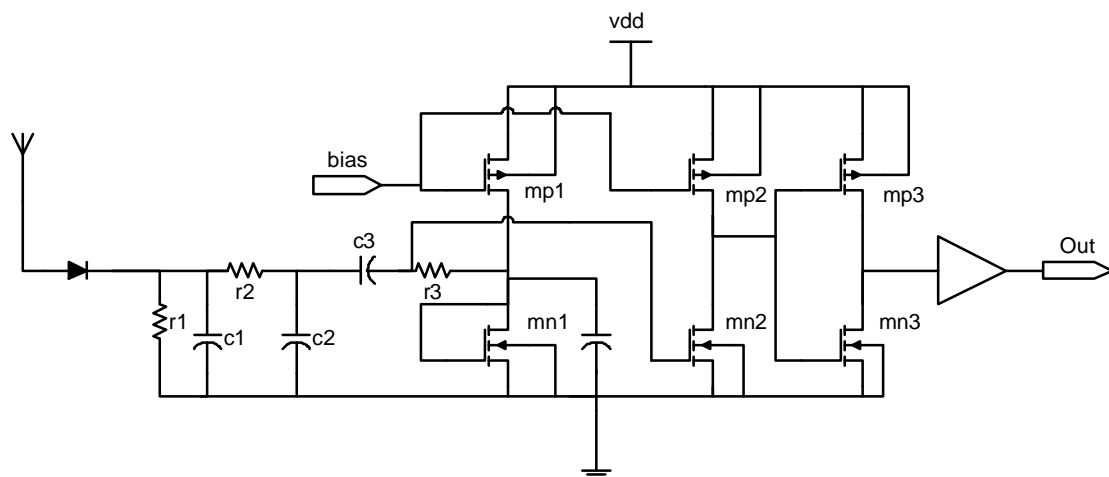


Fig. 15 single transistor amplifier demodulator

### 3.5 Backward Link modulator

As a counterpart of the demodulator, the backward link modulator is another essential part of the RFID analogue front end. In the analysis of the RFID systems it is important to consider whether the labels are placed in the far (propagating) or near (energy storage) fields of the reader (interrogator) antenna. Usually, the working ranges of the HF and UHF RFID systems are different. The HF RFID systems are based on magnetic coupling of magnetic systems. The magnetic coupled communication is only possible if the near field condition:

$$d < \frac{1}{2p} \quad (\text{Equation 3.19})$$

is valid.<sup>xii</sup> By equation 3.19, we can see that the UHF RFID systems are working in the far field. Since the working ranges are different, the coupling operations as well as the backward modulation algorithms are different.

### 3.5.1 HF backward link modulator

The HF systems can be modelled as magnetic coupling system like what we described in section 3.1. From the perspective of the reader (interrogator), the tag is a kind of load. The reader antenna and the tag antenna form a transformer. Ideally, the reader antenna and the tag antenna themselves don't consume any power. The power is consumed by the parasitic resistance as well as the tag IC. If we think the HF RFID simulation model of figure 5 in a different way, we may find some instincts of the coupling between the reader and the tag. We remodelled the HF RFID simulation model of figure 5 to be the one showed in figure 16. The tag is modelled as a impedance  $Z_{load}$  serially connected with the reader antenna and the RC impedance match network of the reader. Since the impedance matching network and the antenna are fixed, the variation of the impedance  $Z_{load}$  will affect the power transfer efficiency. When the impedance  $Z_{load}$  is matched with the network, maximum power can be transferred to the tag. If not, the power will be reflected back to the source. So the back modulation of the HF system is actually a kind of load modulation, which is carried by the modulation of the load impedance.

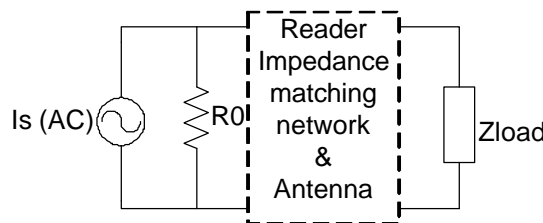


Fig. 16 Equivalent reader model

The impedance has real part and imaginary part. The tags at different physical locations can be modelled as different impedance with different real and imaginary parts. The variation of the impedance  $Z_{load}$  will affect the power transferred to tag and so do the voltage on the  $Z_{load}$  as well as antenna terminals and other network connection nodes. The reader might use the variation of the voltage for the decoding of the backward link signals. We can change impedance  $Z_{load}$  by the real part and/or

the imaginary part. The way to change the real part is modulating resistive load inside the tag chip, and the way to change the imaginary part is modulating capacitance inside the tag chip. The possible implementations are shown in figure 17. Nevertheless, none of the two approaches can purely affect read or imaginary part of the load impedance. The real modulation will always affect both the real and imaginary part at the same time.

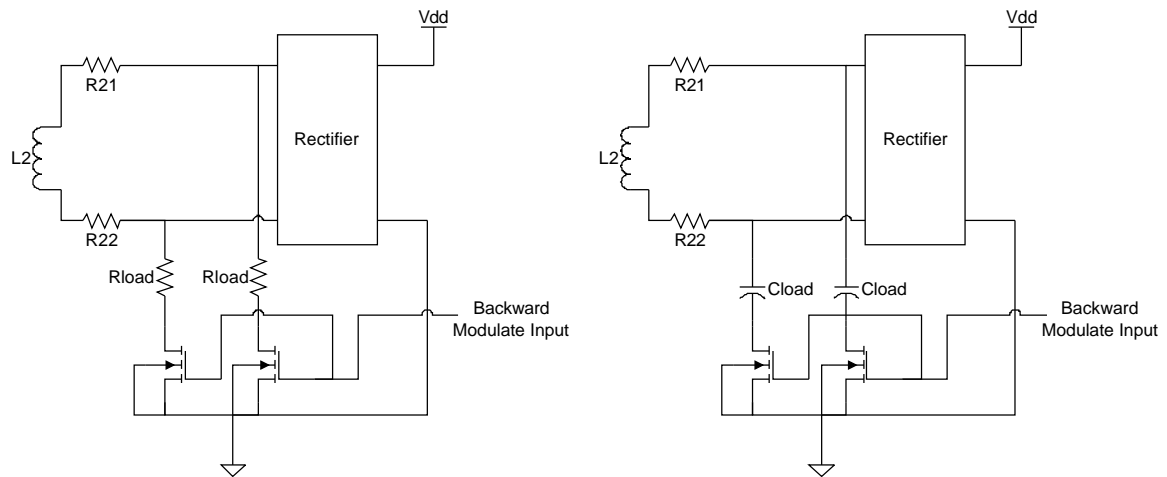


Fig. 17 Load modulation implementations

As we know, the readers may have different structures and antenna designs. At the same time, we have not been able to sort out an appropriate analysis approach to solve the design with good accuracy and reasonably easiness yet. And the ISO/IEC 10373-6 and 10373-7 standards formulate the test method of the HF RFID systems' back modulation depth. The standard regulates a fixed impedance match network and fixed antenna parameters. Then it uses two sensor coils to attenuate the carrier, which is like the twisted pair cable, so as to capture the variation of the back modulation depth. The modulation power is converted to the sensor coil terminal voltage for measurements. So it is more like a practical approach than analytical approach. What we did in our past experience is making several options over the Load resistor or capacitor and modifying the values by testing. What we can suggest to the readers on the parameters of the possible implementations of figure 17 is mostly by our design experience. The MOS transistor parameters do not affect the back modulation depth much. The appropriate value of gain  $b = 5 \sim 10m$ . And the load resistor  $R_{load} = 500 \sim 2k\Omega$ , the load capacitor  $C_{load} = 4 \sim 6pF$ . The readers should do some simulations for your own design. If you use the same parameters as the ISO/IEC 10373 in your simulation model, you may be able to grab the voltage variations at the reader antenna terminal. However, it might be too small to read. It's better to model the sensor coils for higher accuracy, too. Nevertheless, it is still a kind of simulation rather than theoretical analysis. So the most important thing is set up the test benches to check and modify the value after the silicon.

### 3.5.2 UHF backward link modulator

As we know, Electromagnetic waves radiated from the transmitter antenna will meet different target items. Part of the power will be absorbed by the targets, while others will be scattered into different direction with different amplitude. Finally a very small part of the power will be reflected back to the send reader. The UHF RFID systems use this physical approach to fulfil the backward link communication. The back-scattering idea is inherited from Radar terminology.

As we know, the tag is powered by the EM fields radiated by the transmitter antenna. The power, which is received on the tag, depends on many conditions: like the carrier frequency (absorption coefficient of the medium), the temperature, the reflections and/or the moving conditions. So we might start our analysis or tag chip circuits design from the ideal scenario, which is considering the free line of sight, free space attenuation and permanent transmitted carrier.

Since only the reader/transmitter radiates power in the passive UHF RFID system, we can get the power intensity of power flow per unit area of the reader/transmitter to be:

$$S_{reader} = S = \frac{g_{reader\_ant} P_{reader}}{4\pi r^2} = \frac{EIRP}{4\pi r^2} \quad (\text{Equation 3.20})$$

Where  $g_{reader\_ant}$  and  $P_{reader}$  are the gain of the reader antenna and the power which it transmits. The reason we put the EIRP in the equation 3.20 is the fact that EIRP (or ERP) are regulated by regulations while the physical implementations of the readers and antennas might be different.

So the power input to the tag/transponder IC is:

$$P_{tag\_IC} = S_{reader} A_{e\_tag} = S A_{e\_tag} \quad (\text{Equation 3.21})$$

Where  $A_{e\_tag}$  is the effective area of the tag, which is given by:

$$A_{e\_tag} = \frac{g_{tag\_ant} \lambda^2}{4\pi} \quad (\text{Equation 3.22})$$

So, the power input to the tag/transponder IC can be re-written as:

$$P_{tag\_IC} = EIRP \cdot g_{tag\_ant} \left(\frac{\lambda}{4\pi r}\right)^2 = P_{reader} \cdot g_{reader\_ant} \cdot g_{tag\_ant} \left(\frac{\lambda}{4\pi r}\right)^2 \quad (\text{Equation 3.23})$$

It's better for us to understand the relations with some practical mathematical analysis. For example, with the European regulation of EIRP=825mW and carrier frequency is 865MHz, tag antenna gain  $g_{tag\_ant} = 2.15dB = 1.64$ , and the distance is 2m, we can get the input power to the tag IC is:

$$P_{tag\_IC} = EIRP \cdot g_{tag\_ant} \left(\frac{\lambda}{4\pi r}\right)^2 = 0.825 \times 1.64 \times \left(\frac{3 \times 10^8}{4 \times 3.14159 \times 2 \times 865 \times 10^6}\right)^2 = 257 \mu W$$

and the  $P_{tag\_IC} = 64 \mu W$  at the distance of 4 meters.

Considering the rectifier efficiency, the input power to the core circuits will be in the magnitude of several tens of microwatts.

The backward link can be treated with the same relationships as described above. Firstly, we consider the total reflection. If the total incident power received by the tag IC is reflected by, the received power to the reader receiver is:

$$P_{reader\_rec} = P_{reader} \cdot g_{reader\_ant}^2 \cdot g_{tag\_ant}^2 \left(\frac{l}{4\pi r}\right)^4 \quad (\text{Equation 3.24})$$

If we substitute the gains of antennas with the effective area, the received power of the reader receiver is:

$$P_{reader\_rec} = \frac{P_{reader} \cdot A_{e\_tag}^2 \cdot A_{e\_reader}^2}{l^4 \cdot r^4} \quad (\text{Equation 3.25})$$

From equation 3.24 and 3.25 we can see that the reader's receive power is reverse proportional to the four squares of the distance between the tag and the reader. If we double the distance, the received power at the reader would be decreased to 1/16 of the previous one.

If we use the same parameters as the calculation of tag input power, and set the reader antenna gain  $g_{reader\_ant} = 10dB = 10$ , the maximum received power at the reader (tag full reflection) is:

$$\begin{aligned} P_{reader\_rec} &= P_{reader} \cdot g_{reader\_ant}^2 \cdot g_{tag\_ant}^2 \left(\frac{l}{4\pi r}\right)^4 \\ &= 0.0825 \times 10^2 \times 1.64^2 \times \left(\frac{3 \times 10^8}{4 \times 3.14159 \times 2 \times 865 \times 10^6}\right)^4 = 8e-4mW = -31dbm \end{aligned}$$

And the effective area of the tag with the given parameters is:

$$A_{e\_tag} = \frac{g_{tag\_ant} l^2}{4\pi} = \frac{1.64}{4 \times 3.14159} \times \left(\frac{3 \times 10^8}{865 \times 10^6}\right)^2 = 0.0157m^2 = 157cm^2$$

The result seems to be very positive, however, remember the assumption of full reflection and full absorption cannot be achieved in reality. Otherwise, on one hand the chip will not work, on the other hand, even the power to the tag is fully reflected, it will be absorbed or scattered by some other targets before they reach the reader.

Now we might incorporate the differential radar cross-section area  $\Delta RCS$  to formulate the more realistic situations. We apply the radar cross-section area  $\Delta RCS$  to the whole tag rather than the tag IC only.

$$\Delta RCS = \Delta RCS_{tag} = g_{tag\_ant} \cdot \Delta RCS_{tag\_IC}$$

and

$$P_{reader\_rec} = \frac{S_{reader} \cdot \Delta RCS}{4\pi r^2} \cdot A_{e\_reader} = EIRP \cdot g_{reader\_ant} \cdot \frac{l^2}{64\pi^3 \cdot r^4} \cdot \Delta RCS \quad (\text{Equation 3.26})$$

We can see that the reader receive power is directly proportional to the tag differential radar cross-section area  $\Delta RCS$  and the reader antenna gain  $g_{reader\_ant}$ .

Since the antenna impedance is fixed, what we actually do is modulating the impedance of the tag IC to change the radar cross-section area. From this perspective, we might better to analyse the  $\Delta RCS_{tag\_IC}$  than the whole tag radar differential cross-section area  $\Delta RCS$ . The equation 3.23 gives us the incident power to the tag IC. The figure 18 is the equivalent circuit of the tag IC with input power source.

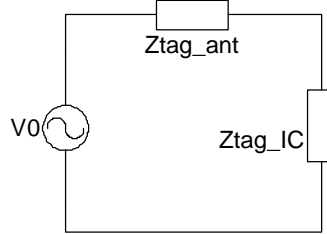


Fig. 18 Equivalent circuit of tag IC with input power source

The available power to the tag IC can be written as:

$$P_{tag\_IC} = \frac{V_{rms}^2}{R_{tag\_ant}} = \frac{V_{p-p}^2}{8R_{tag\_ant}} \quad (\text{Equation 3.27})$$

And the  $P_{tag\_IC}$  value can be calculated from the equation 3.23. As any other power transferring systems, if the  $Z_{tag\_ant} = Z_{tag\_IC}^*$ , which means,  $R_{tag\_ant} = R_{tag\_IC}^*$  and  $jX_{tag\_ant} = -jX_{tag\_IC}$ . Then all the incident power to the tag will be absorbed and the maximum power can be transferred from the tag antenna to the tag IC. We can get:

$$\Delta RCS = g_{tag\_ant} \cdot \Delta RCS_{tag\_IC} = 0$$

With the antenna open or short ( $Z_{tag\_IC} = 0$  or  $Z_{tag\_IC} = \infty$ ), all the power transferred to the tag IC will be reflected back. So the maximum  $\Delta RCS$  will be:

$$\Delta RCS_{max} = g_{tag\_ant} \cdot \Delta RCS_{tag\_ICmax} = A_{e\_tag} \cdot g_{tag\_ant} = \frac{l^2}{4\pi} \cdot g_{tag\_ant}^2 \quad (\text{Equation 3.28})$$

We cannot use the extreme value of  $\Delta RCS$  (0 and  $\Delta RCS_{max}$ ) in real implementations. The amount of reflected signal from the tag IC to the power source (actually back to the air) is dependant on the degree of mismatch between the tag antenna impedance and the load impedance. We use the reflection coefficient, which is formulated by equation 3.29, to define the ratio between the reflected voltage wave and incident voltage wave.

$$\Gamma_L = \frac{V_{ref}}{V_{inc}} = \frac{Z_{tag\_IC} - Z_{tag\_ant}}{Z_{tag\_IC} + Z_{tag\_ant}} \quad (\text{Equation 3.29})$$

The reflected power can be formulated by:

$$P_{tag\_IC\_ref} = \frac{V_{p-p}^2}{8R_{tag\_ant}} \cdot \left| \frac{Z_{tag\_IC} - Z_{tag\_ant}}{Z_{tag\_IC} + Z_{tag\_ant}} \right|^2 = P_{tag\_IC} \cdot \left| \frac{Z_{tag\_IC} - Z_{tag\_ant}}{Z_{tag\_IC} + Z_{tag\_ant}} \right|^2 \quad (Equation 3.30)$$

So the tag differential radar cross-section area between two tag IC impedances  $\Delta RCS_{1,2}$  can be written as:

$$\Delta RCS_{1,2} = g_{tag\_ant} \cdot A_{e\_tag} \cdot \left| \frac{Z_{tag\_IC1,2} - Z_{tag\_ant}}{Z_{tag\_IC1,2} + Z_{tag\_ant}} \right|^2 \quad (Equation 3.31)$$

The actual power available to the tag IC can be given by:

$$P_{tag\_IC\_in} = P_{tag\_IC} - P_{tag\_IC\_ref} = P_{tag\_IC} \cdot \left( 1 - \left| \frac{Z_{tag\_IC1,2} - Z_{tag\_ant}}{Z_{tag\_IC1,2} + Z_{tag\_ant}} \right|^2 \right) \quad (Equation 3.32)$$

By analysing the equation 3.31 and 3.32, we are able to see that we have to check and balance between the reflection and the available power to the tag IC. From the perspective of the powering of the tag IC, it is always better to minimize the reflection. On the other hand, it is better to increase the signal noise ratio of backward link communication by higher reflection. So our approach is getting the differential radar cross-section area or the reflection coefficient from the reader's specification.

As we know, the core reader's specification is generated by the EM regulations and user's requirements. We have done some calculation on the reader received power previously in this section. We might now do some more to get a better understanding of the possible bottlenecks of the system.

Let's assume the reflection portion of the input power to the tag IC is always 10%. With the European regulation and 2m distance, the effective radar cross section is:

$$\Delta RCS = 10\% \cdot A_{e\_tag} \cdot g_{tag\_ant} = 0.1 \times 157 \times 1.64 = 25.75 cm^2$$

The maximum reader received power is:

$$\begin{aligned} P_{read\_rec} &= EIRP \cdot g_{reader\_ant} \cdot \frac{1}{64p^3 \cdot r^4} \cdot \Delta RCS \\ &= 0.825 \times 10 \times \frac{1}{64 \times 3.14159^3 \times 2^4} \times \left( \frac{3 \times 10^8}{865 \times 10^6} \right)^2 \times 25.75 \times 10^{-4} = 8.04e - 5mW = -40.9dBm \end{aligned}$$

If we increase the range to 3 meters, the  $P_{read\_rec} = -48dBm$  and at 4 meters,  $P_{read\_rec} = -53dBm$ . Like what we have said before, the results are got by idealist analysis. As we know, no real application takes place in an anechoic chamber! So we might add another 20dB attenuation of the received power and can get the received power of the reader to be  $-75dBm$  to  $-61dBm$ . It is not very hard to get a receiver with sensitivity higher than  $-80dBm$  nowadays. From this point of view, we may see that the communication bottlenecks still exist on the tag power. At 4-meter distance, the maximum input power to the tag IC is only 64uW with the antenna gain 1.64 (or 39uW with the antenna gain of 0dB). Considering the rectifier efficiency at low input power, it is really a challenge for the chip designer.



### 3.6 Clock Extraction or generation

The digital core has to have the system clock to run the state machine or microprocessor and decode and encode the data. So every RFID tag chip needs a clock generation circuit block and the clock generation is always a part of the RFID front-end.

For the HF (13.56MHz) system, it is easy to extract the clock signals from the carrier and divide down to feed into the digital core. We can use a simple inverter to fulfil the work. The reason why we can use direct extraction in HF system is considering to facts. One is that the data rates compare to carrier frequency is not that small and some of the backward links incorporate sub-carrier, which is even closer to the carrier frequency. So the system clock can got from the carrier by dividing several times, for example, 8 times or 16 times. The other is the comparatively high power budget for the HF systems. As we know, the high the switching frequency, the high the dynamic power. So clock division circuits usually consume large power. And the HF systems can bare the dynamic power consumption raised by the clock extraction or division circuit. Figure 20 shows a certain HF RFID clock extraction circuit. When we implement the circuit, we have to remember two issues. Firstly, we have to decrease the threshold of the input inverter. Since the input of the clock extraction is antenna and the AM modulation will cause the amplitude to drop to very low even zero. And it is better to maintain the clock extraction output for some while at the rising and falling edge of the modulation dip. And during the backward modulation, the antenna amplitude will also be dragged to low. So we'd better to decrease the threshold of input inverter. Secondly, we'd better to make the size of transistors in the first a few stages of frequency division as small as possible. According to  $P_{switch} = \frac{1}{2} \cdot C \cdot V^2 \cdot f$ , we can decrease the transistor size to minimize the capacitor so as the dynamic switching power.

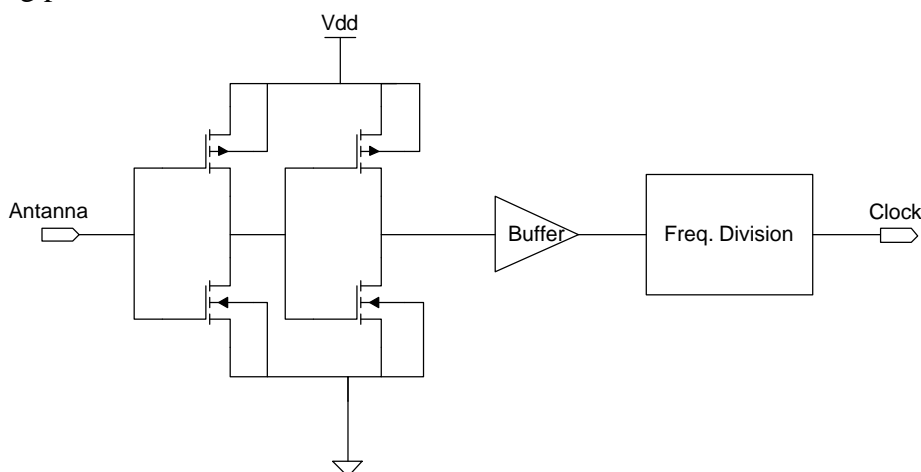


Fig. 20 HF (13.56MHz) Clock Extraction circuit

When we come to the UHF systems, we cannot use the direct extracting approach. The carrier frequency is tens of thousand times higher than the data rate; it is unrealistic to direct divide the carrier down for the digital core because of the

complication and huge power consumption. We have to implement an on chip oscillator to generate the system clock in UHF tag chips. To design an ultra low power fast locking oscillator is not an easy task and has not been explored by us yet. So we will give detailed analysis over it as a separate work of this tutorial. The basic conclusion will be added in once the work is finished.

### 3.7 Power on Reset

Power on Reset circuit has two major functions. One is generate the whole chip reset signal when the tag is powered up by the EM fields. The other is to protect the chip circuit from malfunction when the power supply voltage drops under a certain level.

The POR circuit is a mature analogue building block. The specification of our application does not vary much from the others. The only critical issue is the power consumption of the POR circuit itself. The figure 21 shows an approach of the POR circuit. No matter how different the circuits' implementation might be, the basic idea of the POR circuits is the same. The POR circuit has to sense the power supply level and compare with a certain threshold voltage. If the power supply exceeds the threshold level, the POR circuit will turn on some kind of switches to generate the output signal. Since it is always necessary to have a certain delay between the power available and the reset disable. There is delay circuit in the POR block. In order to make better immunisation of the unstable output states caused by power fluctuation around the threshold, we have to have some hysteresis level mechanism. Since the POR block has to protect the circuit from malfunction as well as to generate the global reset, the voltage sampling and/or the threshold comparison circuits have to work all time. The main quiescent power consumption of the POR is caused by the sampling and comparison. They are the main optimisation objectives.

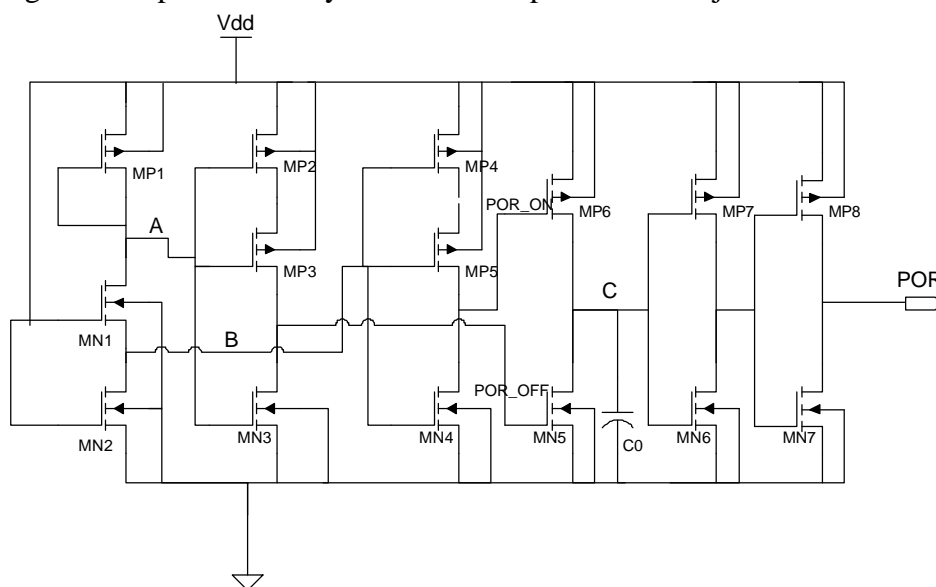


Fig. 21 POR circuit

In figure 21, The MP1, MN1 and MN2 branch is the power level sampling. The MP1 is working in the saturation region, while the MN1 and MN2 are actually forming a transistor, which is working in triode region as a resistor load. The MN1 is used to generate the voltage hysteresis. In order to decrease the quiescent current of this

branch, the MN1 and MN2 must be very small. Let's assume the MN1 and MN2 form one transistor MN1, we can get:

$$I(MP1) = \frac{1}{2} b_{MP1} (V(A) - VDD + V_{tp})^2$$

And the resistor of the MN1 in the triode region can be given by:

$$R_{MN1} = \frac{1}{b_{MN1} (VDD - V_m - V(A))}$$

$$I(MN1) = \frac{V(A)}{R_{MN1}} = I(MP1)$$

Assume  $V_m = -V_{tp} = V_t$  and  $k = \frac{b_{MP1}}{2b_{MN1}}$

$$V(A) = \frac{k}{k+1} (VDD - V_t) \quad (\text{Equation 3.33})$$

From equation 3.33, we can see that the voltage of node A follows up with the supply voltage by a  $V_t$ .

After the voltage levels are shifted down, node A and B are connected with the inputs of two identical invertors separately. The invertor seems a little bit different from the normal one. The MP2, MP3 and MP4, MP5 actually form two very "long" transistors. The reason to do so is to decrease the quiescent current of the two invertors. We use invertor as comparator in this implementation. The switch level of the invertor serves as the threshold. Once the voltage of the input exceeds the switch level, the invertor will be turned on. Since the voltage of input (node A and B) can never reaches up the power supply VDD. The PMOS transistors cannot be switched off. So we have to decrease the beta of these PMOS transistors so as to decrease the quiescent currents. The quiescent currents can be controlled under 100nA or so without much difficulty.

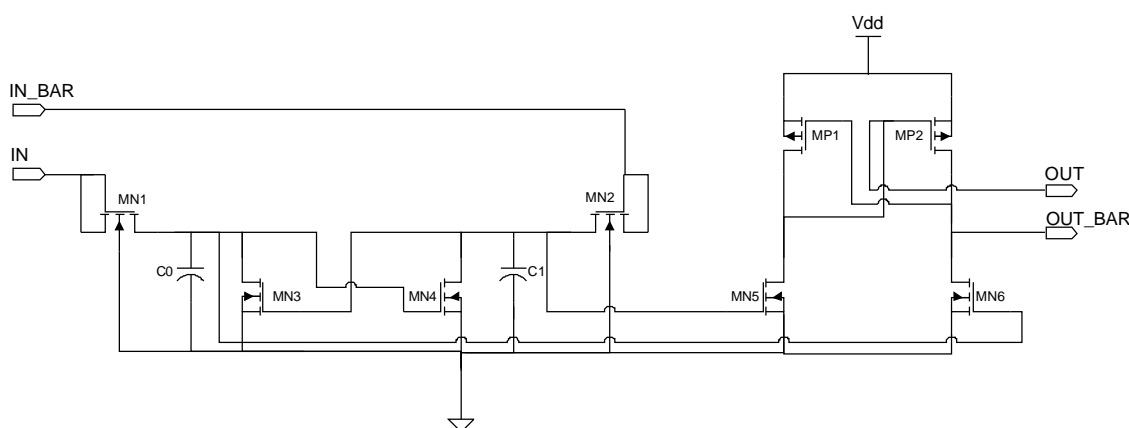
MP6 and C0 form the delay circuit to generate the time delay we need. Since the voltage of node C will ramp up slowly when the supply voltage reaches the Power On threshold. The invertor formed by MP7 and MN6 will remain at the transition state for a while. The time duration when the MP7 and MN6 are both on is determined by the ramp on speed of node C. So it's better to keep the time delay as small as possible for less power consumption. And we decrease the size of the MP7 and MN6 at the same time so as to minimize the switch power. The output invertor is used to increase the gain (fast switch time and large driving capability) and reverse the polarity. We have got the quiescent current of whole POR circuit to be less than 300nA and switch power peak less than 800nA with a common 0.35um CMOS process at the 2V supply level. And we are sure there are rooms for power optimisation over our results. Of course, the quiescent current will go up with the supply level. However, the worse case is for the smallest input power and lowest power supply level.

### 3.8 Short-term memory

Short-term memory (persistent memory or flag) is a kind of memory whose states can be maintained during a brief loss of tag power. Nowadays most of the protocols need

short-term memory to store the identification and/or selection states. So it is worthwhile to give some reference on the short-term memory implementation.

Firstly, the short-term memory is a kind of special memory, it has to store values or states. Secondly, the stored value can be maintained for a short period, rather than non-persistent like SRAM, DRAM or non-volatile memory like EEPROM. The persistent time specification is around several seconds, while the programming time should be less than 1 or 2 ms.. These requirements have outlined the basic specification for the short-term memory. Figure 22 presents our short-term memory approach.



*Fig. 22 An approach of short-term memory*

Actually, the core of the short-term memory is similar to 4-T SRAM as shown in the left part of the figure. The right part is the level shifter as well as output stage to recover from the threshold loss that is caused by MN1 and MN2 and present the output drive. The short-term memory uses differential input. The capacitors C0 and C1 are used to maintain the value between power-loss. The reason we have to use the differential input (symmetrical structure) is that the maintain time is several seconds and the programming time should be less than 1 or 2 ms.. If we want to program state "1", the IN will be "Vdd" and the IN\_BAR will be zero, the capacitor C0 will be charged up. Once the voltage reaches up the threshold voltage of the MN4, the capacitor C1 will be discharged quickly and the value will be retained through positive feed-back. During power-loss, both of the inputs will be reset to zero. We can use two registers with reset function to feed in the programming inputs. Once the power level drops under the power-off threshold, which is still high enough for the logic function, the programming input will be reset to zero and protect the inside states untouched by the reverse biased MN1 and MN2. Since the charges stored on the capacitor can only be discharged by two reverse biased NMOS transistors and substrate leakage, the charges can be retained for a long time. The maintain time depends on the size of transistors and the manufacturing processes. The readers have to do some test and verification to find out the appropriate capacitor value and transistor sizes to meet the requirements.

Once the tag is re-powered up, the IN and IN\_BAR will still remain zero after power on reset. And if the storage node voltage has not decayed under the threshold voltage



of NMOS transistors MN5 or MN6, the outputs will be re-established or restored. The state-machine or the Micro-controller program will read the output of the short-term memories and refresh or reprogram according to the specification.

Like the POR and any other circuits in the RFID tag chip, the power consumption of the short-term memory is a critical task for the design. The major power consumption of the memory is during the programming and refreshing. And besides the level shifter switching power, the most of the power is consumed by charging capacitors while the feedback transistors are still on, which forms a kind of short cut between the power supply and the ground of chip. So we have to carefully design the size of the input transistors MN1 and MN2 as well as the size of MN3 and MN4 in our proposed approach. Fortunately, the programming speed of the RFID application is much slower than the application like SRAM and DRAM. We might be able to sacrifice the programming speed to meet the power budget.

### 3.9 Other circuits

The RFID front end has to incorporate some other circuits besides the ones we have talked about. The most probable one would be voltage (current) reference circuit. The reference circuit for the RFID front end has several specific specifications that are different from normal reference circuit. One issue, the power-supply level. Before the other circuit blocks can function correctly, like the regulator, the reference should be established. So the minimum supply level maybe under 1.5Volt. The other is the power consumption of the reference circuit itself. In RFID applications, 0.1Volt voltage variation might be acceptable while 10uW power consumption is unbearable. The paper<sup>xiii</sup> has present some ideas on the low-power supply voltage reference.

Like the on-chip oscillator, we have not explored too much on the RFID voltage (current) reference circuit, we will not give detailed analysis in this tutorial. We will incorporate this in our later revisions.

Besides the reference circuit, there are other circuit blocks as well as structures in the RFID front end. For example, the ESD protection, antenna bonding structures, etc. These blocks or structures are as important as the one we have analysed in detail. The readers should not omit them or treat them coarsely.

## 4. Summary and Acknowledgements

Considering the importance of the RFID tag/transponder front-end in the RFID technology and the reality that no suitable and detailed materials have published on it, we presented this tutorial paper. We presented the front-end architecture that is probably versatile in all RFID tag chip. And we give detailed analysis over the circuit blocks, like the rectifier, regulator, demodulator, modulator, clock extraction, POR, etc. Besides the structure of the circuit blocks, we also presented the ways to get the device parameters according to the system specifications. Most of the structures we presented in this tutorial are proven by our previous works and others' publication.



We hope to give the readers an overall image of what is the RFID tag/transponder chip analogue front-end and how to implement it from scratch.

There must be some errors or misunderstandings in this tutorial. The readers are encouraged to verify the ideas by simulation as well as experiments. We found that it is always better to analyse by you rather than take everything in by the others.

There is an old saying in Chinese: “Throw out a brick to attract a jade” which means we offer a few commonplace remarks by way of introduction and hope to raise the interests and come up with some valuable opinions by everybody’s efforts finally.

The author would like to give thanks to Mr. David Hall of Tagsys for his contribution on the Matlab signalling script and the regulator circuits, to Ms. Yin Liu of Shanghai Huahong IC. for her contributions on the HF simulation models. And the author would like to give thanks to Professor Peter H. Cole for his support and supervision. Last but not least, the author would like give thanks to the colleagues Kinseong Leong, Munling Ng, Ben Jamali and Damith Renasinghe for their support and valuable comments.



## Annex A

### Sample MATLAB script for the filter and data envelop generation

\*Note: this is only an example; the data rate, encoding scheme as well as other parameters are subject to change.

```
% Written by David. Hall and modified by Kinsong and Zheng
% 1 jul 2004 pie for europe with 3kHz(6dB) rbw
% out of band 30dB down for out of band bw of 200kHz, fc+/-100kHz
% out of band 69dB down for out of band bw of 400kHz, fc+/-200kHz
clg
clear
pack

tari=10e-6;
rrate=320e3;

%dip=80% AM index
dip=80;
v_amp=1-dip/100;

fs=10e6;
T=1/fs;

t_w=tari/2;
t_slot=2*t_w;
t_extra=t_w;
n_slot=fix(t_slot/T)+1;
n_extra=fix(t_extra/T)+1;

%raised cosine
%t_low=t_w; %pulses
%n_low=fix(t_low/T)+1;
%v_data1=v_amp+dip/100*(1+cos((0:n_low-1)*2*pi*T/t_low))/2;
%n_space=n_slot-n_low;
%square pulse to check theory
t_low=t_w;
n_low=fix(t_low/T)+1;
v_data1=v_amp*ones(1,n_low);
n_space=n_slot-n_low;

t_rbit=1/rrate;
n_rbit=fix(t_rbit/T)+1;
v_wait=ones(1,n_rbit);
v_tag=ones(1,(6+4+96+16)*n_rbit);
v_precursor=ones(1,8*n_rbit);
v_window=ones(1,fix(25e-6/T)+1);

v_space=ones(1,n_space);
v_extra=ones(1,n_extra);
v_slot=ones(1,n_slot);

plot(T*(0:size(v_data1,2)-1),v_data1);
pause

%carrier there
v_0=[v_data1,v_space]; %right
v_1=[v_space,v_data1];
v_sof=[v_data1,v_space,v_data1,v_space,v_slot,v_slot];
v_eof=[v_data1,v_space,v_slot,v_slot,v_slot]; %no more
delimiter=[v_amp*ones(1,fix(12.5e-6/T)+1)];

plot(T*(0:size(v_0,2)-1),v_0);
pause
plot(T*(0:size(v_1,2)-1),v_1);
pause
plot(T*(0:size(v_sof,2)-1),v_sof);
pause
plot(T*(0:size(v_eof,2)-1),v_eof);
pause
```



```
%v_zero_pulse=[v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0,v_0];
%v_ack=[v_slot,v_slot,v_slot,v_slot,v_sof,...
%v_0,v_0,v_1,v_0,v_0,v_0,v_1,v_1,v_1,v_1,v_1,v_1,...
%v_eof];

v_ack=[v_slot,v_slot,v_slot,v_slot,delimiter,v_slot,...
v_slot,v_space,v_0,v_0,v_0,v_0,v_slot,v_0,v_0,v_0,...
v_1,v_1,v_1,v_1,v_1,v_1];
v_cont=[v_window,v_0,v_0,v_slot,v_slot];%discard

v_soh=[ones(1,fix(50e-6/T)+1)];

%ack tag, ack tag, ack notag
v_zero_pulse=[v_soh,v_ack,v_wait,v_tag,v_window,...
v_soh,v_ack,v_wait,v_tag,v_window,...
v_soh,v_ack,v_window];

plot(T*(0:size(v_zero_pulse,2)-1),v_zero_pulse);
pause

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%calc fft of filter, H(k);

fc=1/tari; %the hi and lo of a 0 symbol are considered as unique bits
alpha=0.8;
tr=fc*2*alpha;

taps=128;
h=firrcos(taps,fc,alpha,fs,'rolloff');

%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%need 10ms work of pulse train to get 100Hz resolution in the frequency domain
v_z_temp=v_zero_pulse;
while size(v_z_temp,2)*T < 10e-3,
v_z_temp=[v_z_temp,v_zero_pulse];
end

v_zero_pulse=v_z_temp;
plot(T*(0:size(v_zero_pulse,2)-1),v_zero_pulse);
pause

v_orig=[ones(1,taps/2),v_z_temp]; %see a version before any filtering

v_zero_pulse=conv(v_zero_pulse,h); %add filter

plot(T*(0:size(v_orig,2)-1),v_orig,'r-');
hold on
plot(T*(0:size(v_zero_pulse,2)-1),v_zero_pulse,'b-');
axis([0 30*tari -0.2 1.2])
hold off
pause

clear v_z_temp;
clear v_orig;
N=size(v_zero_pulse,2) %if N is odd it takes a long time
if rem(N,2)~=0
N=N-1
end
resolution=fs/N
X=fft(v_zero_pulse,N);
Pxx=X.*conj(X)/N;
if min(Pxx) == 0
Pxx=Pxx+1e-10;
end

%set up plot
f_limit=500e3;
nf_limit=fix(f_limit*N/fs)+1;
```



```
f=fs/N*(0:N/2);

hold on

plot(f(1:nf_limit),10*log10(Pxx(1:nf_limit))-10*log10(Pxx(1))); %normalise

%set up limit lines
f100=100e3;
n_f100=fix(f100*N/fs)+1;
f125=125e3;
n_f125=fix(f125*N/fs)+1;
f200=200e3;
n_f200=fix(f200*N/fs)+1;

plot(f(n_f100:n_f200),...
(max(10*log10(Pxx(1:n_f100)))-10*log10(Pxx(1))-30)...
-39*((n_f100:n_f200)-size((n_f100:n_f200),2))/size((n_f100:n_f200),2),'r-')

plot(f(n_f200:nf_limit),...
(max(10*log10(Pxx(1:n_f200)))-10*log10(Pxx(1))-69)...
*ones(1,size(f(n_f200:nf_limit),2)),'r-')

[W,H]=max(10*log10(Pxx(2:n_f100)));
text(fs*(H)/N,max(10*log10(Pxx(2:n_f100)))-10*log10(Pxx(1)),...
num2str(max(10*log10(Pxx(2:n_f100)))-10*log10(Pxx(1))))
[Y,I]=max(10*log10(Pxx(n_f100:nf_limit)));
text(fs*(I+n_f100)/N,max(10*log10(Pxx(n_f100:nf_limit)))-10*log10(Pxx(1)),...
num2str(max(10*log10(Pxx(n_f100:nf_limit)))-10*log10(Pxx(1))))
[Z,J]=max(10*log10(Pxx(n_f200:nf_limit)));
text(fs*(J+n_f200)/N,max(10*log10(Pxx(n_f200:nf_limit)))-10*log10(Pxx(1)),...
num2str(max(10*log10(Pxx(n_f200:nf_limit)))-10*log10(Pxx(1))))
[A,K]=max(10*log10(Pxx(n_f125:n_f200)));
text(fs*(K+n_f125)/N,max(10*log10(Pxx(n_f125:n_f200)))-10*log10(Pxx(1)),...
num2str(max(10*log10(Pxx(n_f125:n_f200)))-10*log10(Pxx(1))))

grid
axis([0 f_limit -75 0])
text(0,5,num2str(dip))
text(50e3,5,num2str(tari/1e-6))
text(100e3,5,num2str(rrate/1e3))

hold off
pause

%do single side band modulation
a=v_zero_pulse(1:5000);
abar=imag(hilbert(a));
%carrier cycle 400 so the carrier freq is 1.25MHz
fc=400;
%carrier cycle maximum number is less than 2500, or 5MHz
%fc=1000;
d=size(a);
t=1/d(2):1/d(2):1;
c=cos(2*pi*fc*t);
c90=cos(2*pi*fc*t - pi/2);

%manipulation
upper=1/2.*a.*c;
lower=1/2.*abar.*c90;

result=upper-lower;
resultl=upper+lower;

plot(T*(0:size(resultl,2)-1),2*resultl,'r-');
hold on
plot(T*(0:size(result,2)-1),2*result,'g-');

pause

% call the function to output the data points to a csv file
cell2csv('data_env.csv',a,',');
```



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```
% call the function to output tht data points to timed spice PWL format  
cell2spicepwl('data.sp',a,T);
```



## Annex B

### MATLAB script of matrix value output to spice function

```
% written by Zheng
function cell2spicepwl(datName,cellArray,timestep)
% Writes Cell-Array content and add timesteps to form a spice PWL waveform
%
% datName = Name of the file to save. [ i.e. 'text.csv' ]
% cellarray = Name of the Cell Array where the data is in
% timestep = The timestep between each nodes, usually the 1/sample_rate

% by Zheng Zhu, Auto-ID lab @ University of Adelaide, 2004

datai = fopen(datName,'w');
for z=1:size(cellArray,1)
    for s=1:size(cellArray,2)

        var = eval(['cellArray(z,s)']);

        if size(var,1) == 0
            var = '';
        end

        time=timestep*(s-1);
        if isnumeric(time) == 1
            time = num2str(time);
        end

        if isnumeric(var) == 1
            var = num2str(var);
        end

        fprintf(datai,time);
        fprintf(datai,' ');
        fprintf(datai,var);

        if s ~= size(cellArray,2)
            fprintf(datai,',');
        end
        if s/20==round(s/20)
            fprintf(datai,'\n');
            fprintf(datai,'+');
        end
    end
    fprintf(datai,'\n');
end
fclose(datai);
```

### Spice excitation sample

```
*exitation of the antenna 0.5 is maximum amplitude in this example
Eantenna air 0 vol='0.5*v(t1)*sin(signalfreq*2*3.14159*TIME)'
```

\*data envelop imported from the Matlab script and function output, for example, the 'data.sp' generated by the Annex A script

```
vdata t1 0 pwl(
+0 -0.0011963,1e-007 -0.0023979,2e-007 -0.0035944,3e-007 -0.0047746,4e-007 .....
```



- 
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