

Brief Comparison of Different rectifier structures for HF and UHF RFID (Phase II Draft version 0.0)

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Background

We have compared seven different kinds of rectifier structures in our phase I research. We have found out that no one of the seven different rectifier structures can be used to generate a power of 1.5V on a 45K ohm load with the total power dissipation (available power from air) less than 90uW. The best power consumption index is achieved by NMOS and PMOS gate cross-connected structure (MOS transistor feature size is $W/L=10\mu/0.6\mu$ and $M=2$). And the input level should be around 2.0 volt to get the output DC voltage level in this rectifier structure. And the lowest input voltage level is achieved by 5 stage NMOS charge pump structure while its power dissipation is the largest of all the rectifier structures.

In the phase II research, we plan to focus on the cause of PCE difference especially of those structures with comparatively low PCEs. Then, we will incorporate the discrete Schottky diode model to our rectifier structures. We plan to build simple antenna and tag input impedance model so as to investigate the actual power issues on the RFID tag. We hope to find out the physical constrains on the rectifier structures as well as circuit elements by researching the behavior of the antenna, impedance matching network and the tag. Finally, we plan to present an optimal structures considering the physical constrains and the PCE.

Simulation and Analysis

The simulation and analysis work include:

- (1) Analysis of the cause of the PCE differences;
- (2) Analysis of the PCE relationship with the stages in the NMOS charge pump rectifier structure;
- (3) Build up simple antenna and tag model;
- (4) Analysis of the physical constrains on the rectifier structure;
- (5) Analysis of the PCE of the rectifier structures with discrete Schottky diode model;
- (6) Build up an optimal rectifier structure for solid-state circuits;

(1) Analysis of the cause of the PCE differences

We have simulated and compared the PCE of seven different rectifier structures in the first phase research. The variation of the PCE value among different rectifier structures is big. The cause of the PCE differences is one of the keys to the better rectifier structure design. So firstly, we analyzed the PCE cause in our second phase research.

(1.1) PCE revisited

In the conclusion part of the phase I comparison results report, we have based our comparison on the case of driving fixed load at a fixed DC voltage level. The comparison results are shown in table 1.1 and table 1.2. Now we take in more comparisons based on the simulation results. Table 1.3 and table 1.4 are the comparison results of different rectifier structures on the case of fixed total power consumptions.

	CSM08 diode	CSM06 diode	NMOS brg	NMOS cc brg M=10	PMOS brg M=10	PMOS brg M=2	PMOS cc brg M=10	PMOS cc brg M=2	NMOS PMOS compli	5 stage NMOS chrg pump
Input Level	>3V	>3V	>3V	2.8	3	>3	2.4	2.52	1.9	1.4
Vp-p	>3V	>3V	>3V	2.8	3	>3	2.4	2.52	1.9	1.4
Total Power dissipation	-	-	-	2.51E-04	9.96E-05	-	3.16E-04	1.30E-04	1.12E-04	4.66E-04
PCE	-	-	-	21%	51%	>48%	16%	37.30%	46%	11%

Table 1.1 1.5V, 45Kohm load Minimum input level

	CSM08 diode	CSM06 diode	NMOS brg	NMOS cc brg M=10	PMOS brg M=10	PMOS brg M=2	PMOS cc brg M=10	PMOS cc brg M=2	NMOS PMOS compli	5 stage NMOS chrg pump
Input Level	>3V	>3V	>3V	>3	>3	>3	>3	>3	3	2.0
Vp-p	>3V	>3V	>3V	>3	>3	>3	>3	>3	3	2.0
Total Power dissipation	-	-	-	-	-	-	1.14E-3(at 1.93V)	-	9.71E-04	4.67E-03
PCE	-	-	-	-	-	-	40.8%	-	53.3%	10.7%

Table 1.2 2V, 8Kohm load Minimum input level

Power consumption	CSM08 diode *	CSM06 diode *	NMOS brg M=10	NMOS cc brg M=10	PMOS brg M=10	PMOS cc brg M=10	PMOS brg M=2	PMOS cc brg M=2	NMOS PMOS compli	5 stage NMOS chrg pump
50uW	>58%#	>37%#	42%	13%	40.4%	20%	38%	35%	65%	<4%
100uW	-	-	45.4%	15.7%	51.5%	18%	>48%	36.8%	47%	4.7%
250uW	-	-	-	21%	-	15.5%	-	>39.2%	30.7%	8.2%
500uW	-	-	-	-	-	15.5%	-	-	21.5%	12%

Table 1.3 PCE at different power consumption (45K ohm load)

Power consumption	CSM08 diode *	CSM06 diode *	NMOS brg M=10	NMOS cc brg M=10	PMOS brg M=10	PMOS cc brg M=10	PMOS brg M=2	PMOS cc brg M=2	NMOS PMOS compli	5 stage NMOS chrg pump
50uW	37%	24%	13%	16.5%	15%	28%	13%	22%	38%	<2.3%
100uW	48%	>32%	20.6%	21%	22%	32.6%	20.3%	32.6%	55%	<2.3%

250uW	-	-	32.7%	28.4%	35.8%	36%	33%	42.5%	65%	2.5%
500uW	-	-	-	34.5%	47%	38%	45%	48.5%	62%	3.5%

Table 1.4 PCE at different power consumption (8K ohm load)

*Note: The PCE for the single diode rectifier will be different from the real case. This is because the negative period of the voltage input will only draw a little leakage current and make the power dissipation of the negative period quite small.

'>' and blank areas mean that the total power consumption for the maximum input voltage level (3V) can not reach the proposed value.

The lines of blue shade are of our interests.

Only look at the table 1.3 and 1.4 would be misleading for us to get the merits of the rectifier structures. We have specific needs and constrains of the rectifier. One is the output voltage level, which is minimum 1.5Volt for a common process. The other is the output load, which is around 45K ohm considering the reasonable design overhead. That means the output power should be larger than 50uW. If we add on this constrain and review the table 1.3 again. We will find that the high PCE at low output voltage and power level is useless for real application. For example, the PCE of NMOS and PMOS complimentary structure at total power dissipation of 50uW is 65% does not mean it is better than the others. As we learned from the phase I results, the best PCE for 45K ohm load is achieved by PMOS bridge rectifier. The report of phase one has also pointed out that the minimum input voltage level can be achieved by charge pump structure and the minimum total power dissipation can be achieved by NMOS PMOS cross-coupled structure (not exactly for the case of 45k ohm, just comparatively good considering the PCE and input voltage level). If we increase the load from 45K ohm to 8K ohm, the output power should be larger than 280uW for a 1.5Volt power supply voltage and more than 500uW for 2 Volt power supply voltage. That means the PCE value with total power consumption less than 300uW (500uW for 2V) is not applicable. If you want to make use of the comparative high PCE at the low power consumption region, you have to make the chip work under lower voltage level than 1.5V so as to remain the output currents.

Therefore we have revisited the PCE by giving the two new tables. So we are able to raise questions to investigate on the cause of PCE differences. Our interested questions are:

- (1) The PCE are lower for the gate cross-connected structures than their normal counterparts at light load (for example, 45K ohm) while PCE are higher for the gate cross-connected structures than their normal counterparts at heavy load (8K ohm in our simulation). What's the reason for this?
- (2) The PCE of PMOS gate cross-connected bridge with multiple of 2 is much higher than the one with multiple of 10. What's the reason for this?
- (3) The PCE of NMPS and PMOS gate cross-connected bridge rectifier structure show a very interesting phenomenon: the PCE goes down sharply with the increase of input voltage level for light load (this is not clear for heavy load). What's the cause of it?
- (4) The structure of 5 stage NMOS charge pump rectifier structure seems useless because of its low PCE. What are the causes of the low PCE?
- (5) The ways to improve the PCE of these available structures.

(1.2) Transient analysis MOS transistor model

Since the core part of the rectifier structure is the MOS transistors. It is essential for us to evaluate the transient analysis MOS transistor models to find out the possible cause of the low PCE. HSPICE uses three equivalent circuits in the analysis of MOSFETs: DC, transient, and AC and noise equivalent circuits.¹ We use transient analysis to calculate the power consumption as well as the PCE of the rectifiers. So we take the transient equivalent circuit for our analysis. The figure 1 is the transient equivalent circuit of the (N)MOS transistor.

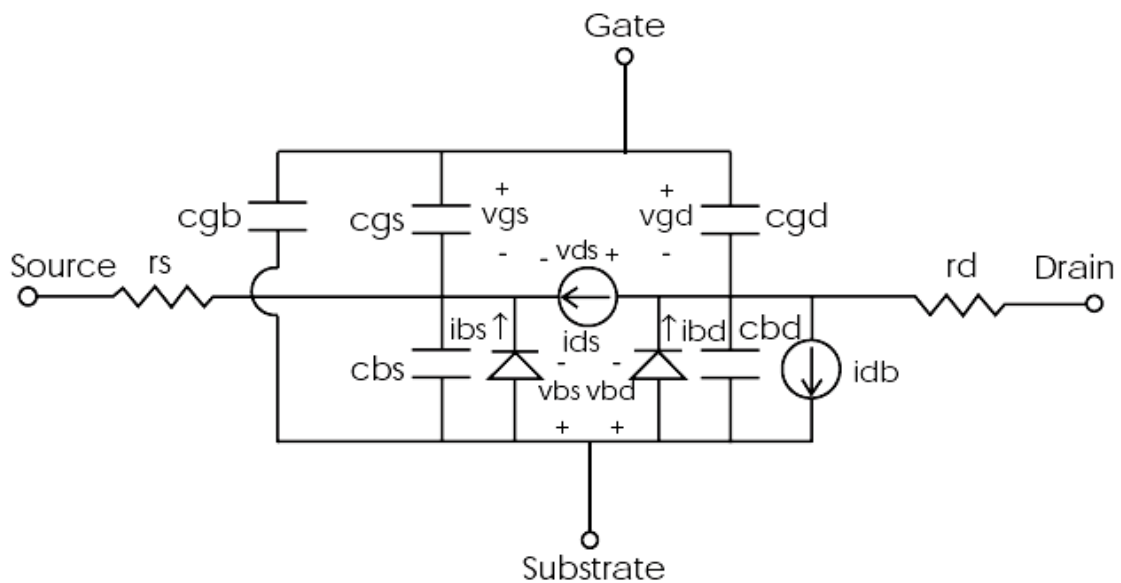


figure 1 MOS transient equivalent circuits

Since we do not take the storage power of the capacitor into calculation when we calculate the total circuit power consumption. The only power consuming elements in the equivalent circuits are: r_s , r_d , substrate-drain diode, substrate-source diode, and channel resistor. The r_s and r_d are source and drain connection resistors, which are treated to be zero in our simulation circuit elements model. So the power is consumed by the NMOS channel resistor and the MOS diodes besides the load resistor. If you want to increase the PCE, you have to decrease the channel resistance. However, the decrease of the channel resistance always introduces larger MOS diodes and the capacitor values. There is always a check and balance.

(1.3) Gate cross-connected structure vs. normal structure

The first question come across is why the gate cross-connected structures have worse PCE than the normal structures at light load and why it is not for the case of heavy load. The advantage of the gate cross-connected one is the smaller turn on voltage and thus the higher output voltage level under same input swing level. And people use this structure widely in HF RF interface circuits for this advantage. However, it looks not as good as it

thought to be for light load (at UHF frequency range with large diode size). In order to find out the cause, we compared the transient models of normal MOS transistor rectifiers with the ones of gate cross-connected. Here, we use NMOS structure as an example. The figure 2 shows the normal NMOS transistor bridge rectifier transient equivalent circuit. And the figure 3 shows the gate cross-connected NMOS transistor bridge rectifier transient equivalent circuit. We model the current source of i_{ds} to be a resistor in our equivalent circuits in these figures. So we should keep in mind that the resistor is **only available** while the transistor is turned on. If the transistor is not turned on, the resistor value is fairly large and can be treated as disconnected.

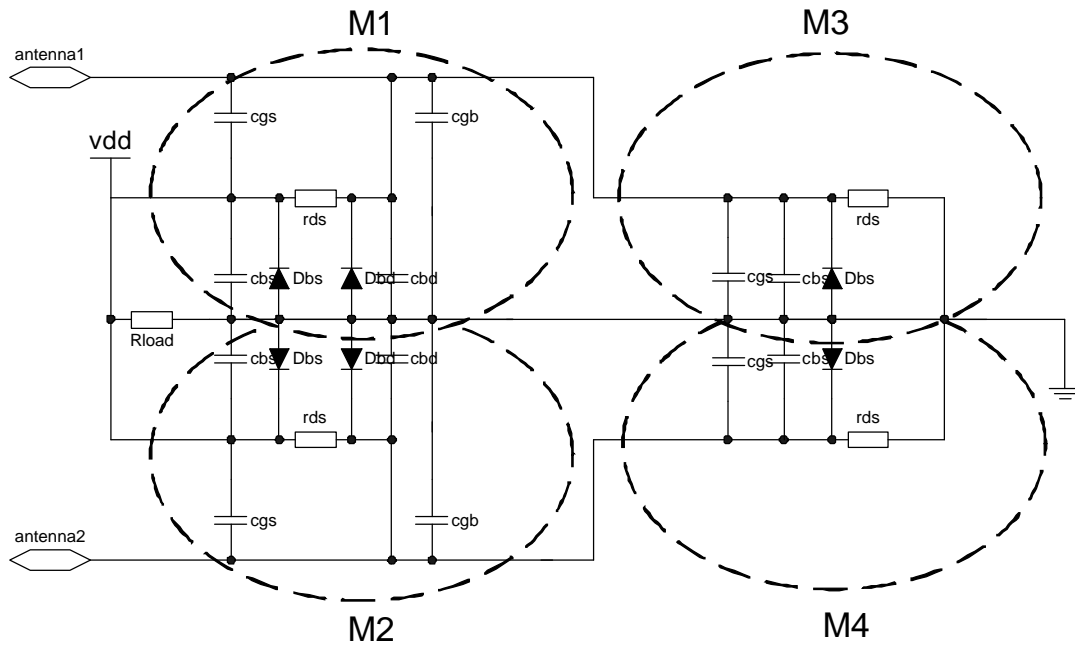


figure 2 normal NMOS bridge rectifier transient equivalent circuit

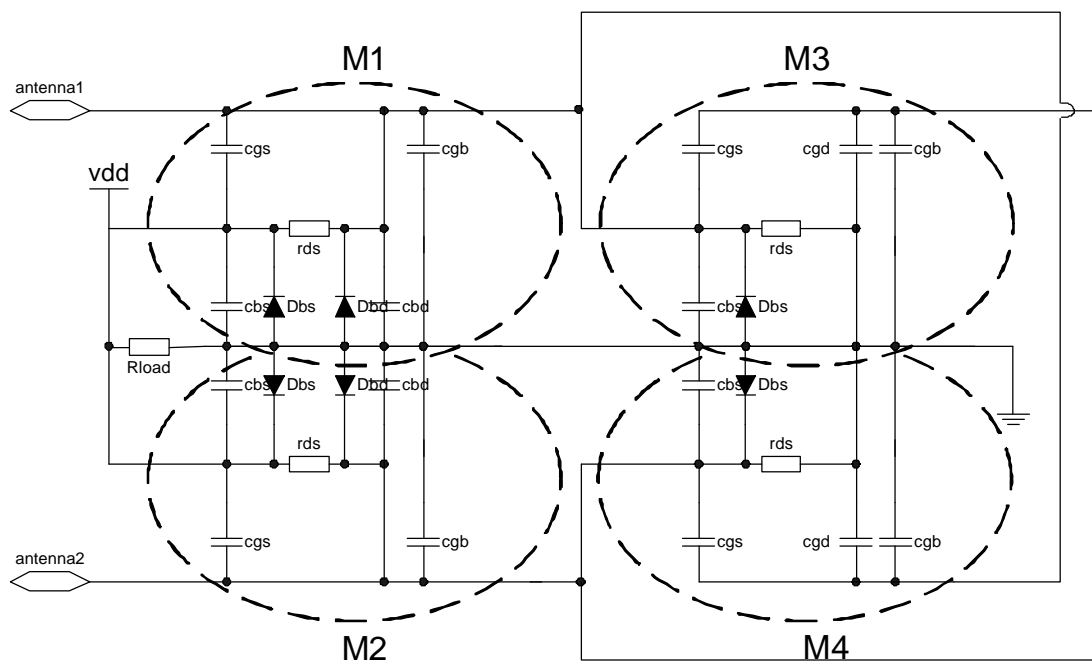


figure 3 gate cross-connected NMOS bridge rectifier transient equivalent circuit

In order to get high PCE, we have to decrease the power consumption on the channel resistor r_{ds} and the substrate leakage of the MOS transistor diodes. The M1 and M2 are same for both the structures. So we consider the M1 and M2 firstly. Since v_{dd} is always higher than gnd , the transistor diode D_{bs} (diode connected between substrate and source) of M1 and M2 are always off. And if we suppose that the turn on voltage of the MOS transistors is higher than the MOS diode's, then the diodes D_{db} of M1 or M2 as well as the D_{ds} of M4 or M3 are on when the antenna voltage is lower than gnd for diode threshold voltage. Thus we have leakage branch of two diodes at every half cycle. However, if the turn on voltage of the MOS transistor M3 or M4 is lower than the MOS diodes, then all the MOS diodes are off and there are no forward bias conductions at all. The r_{ds} of M3 or M4 is available only for short period of time to let the current flow back to the source in this structure. Once the r_{ds} is turned on, the voltage polarity across the r_{ds} is determined. The current always flow from gnd node to antennas through the channel of M3 and M4 for the normal bridge rectifier. Of course, there are currents flows through MOS capacitors (C_{gs} , C_{gb} , C_{bs} , etc.) so as to change the node voltage. Since the element model doesn't include any resistance of these capacitors, Hspice will not calculate the storage energy of these capacitors. In reality, if we taken the resistance into account, there should be more power wasted on the MOS transistors than we have calculated by now.

However, the situation is different in the gate cross-connected case. Because that the transistors M3 or M4 will be turned on if the antenna voltage is higher than the gnd for a threshold voltage. The current flow through the channel will be in different direction according to the voltage polarity of V_{ds} . Figure 4 and 5 shows one of the channel current direction possibilities. The two channels of M3 and M4 cannot be turned on concurrently because of the avoidance of short circuit. The figure 4 shows the condition when the voltage of antenna1 is going up and the antenna2 is going down while still higher than gnd . The figure 5 shows the condition while the antenna1 is going down and the antenna2 is going up.

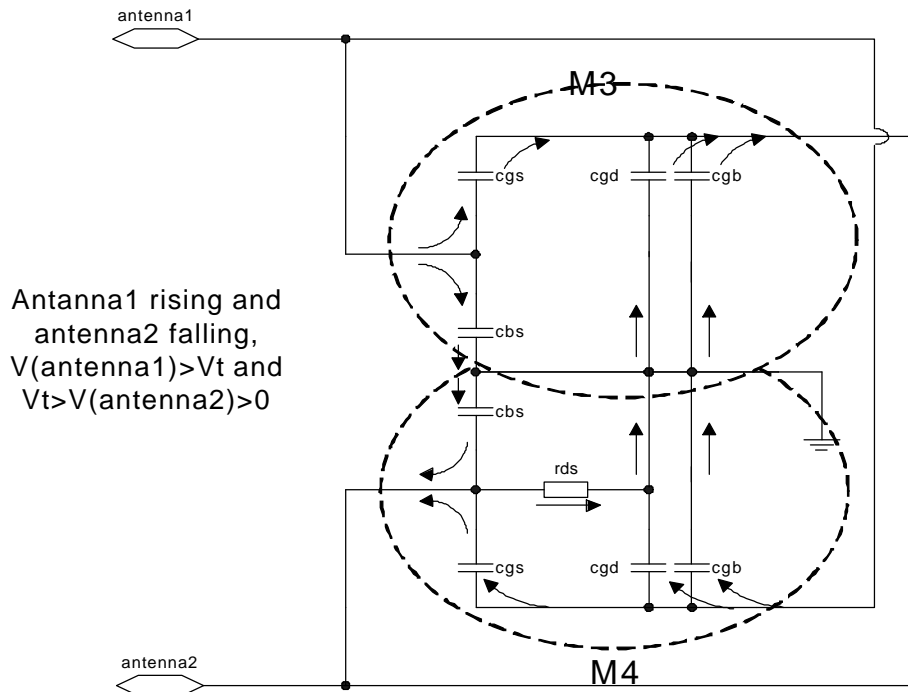


figure 4 current direction in M3 and M4 of the gate cross-connected bridge rectifier
 (condition: antenna1 rising and antenna2 falling)

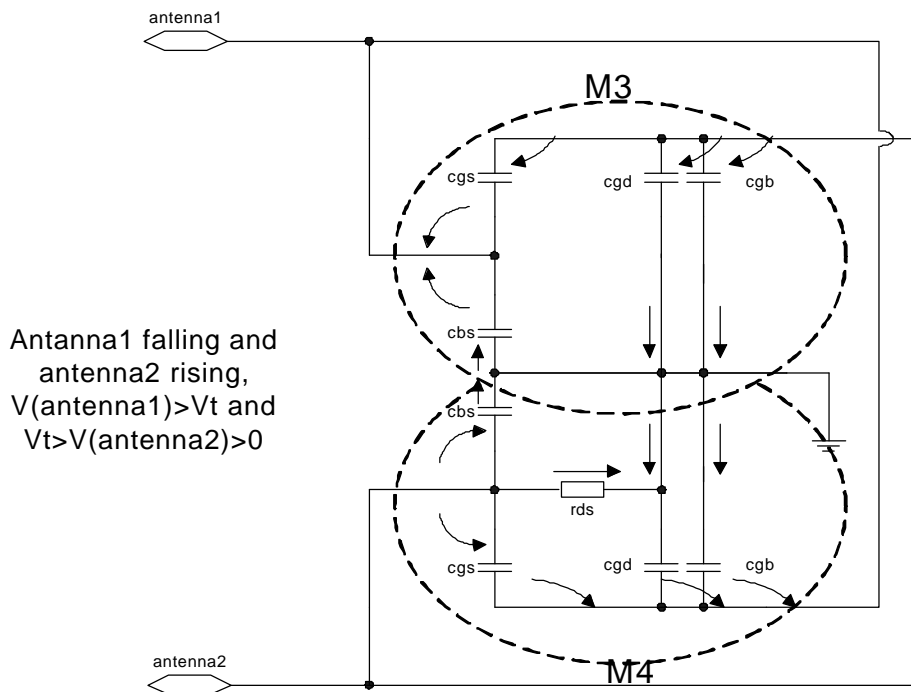
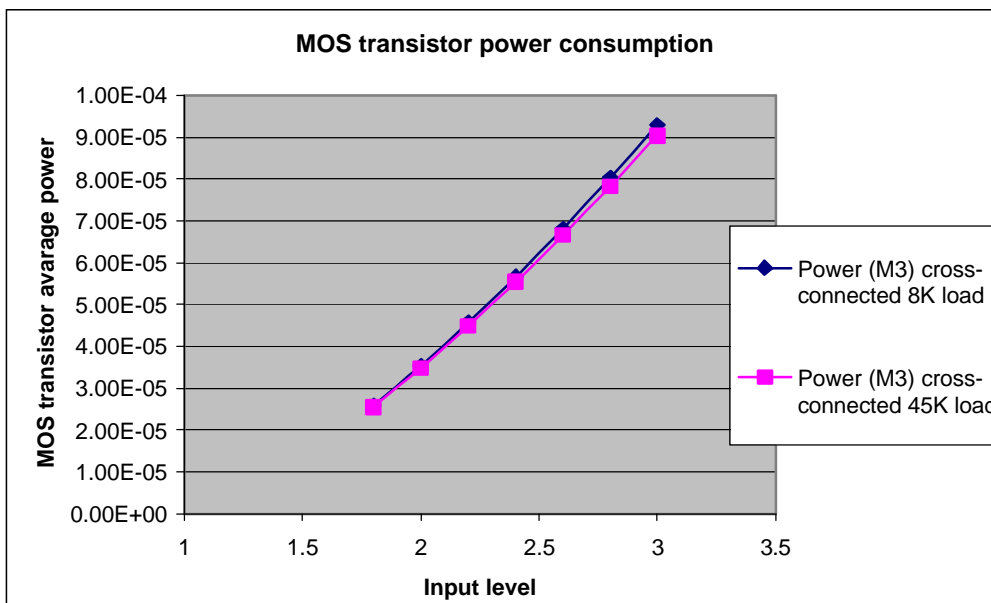


figure 5 current direction in M3 and M4 of the gate cross-connected bridge rectifier
 (condition: antenna1 falling and antenna2 rising)

We can see that the current flow of M3 or M4 channel (through rds) is from antenna2 to gnd and to antenna1. The other current direction is just like the normal bridge rectifier and easy to understand. We can learn from figure2 and 3 that if we want to maximize the PCE we have to make as much current flow between antenna1 and antenna2 are going through the roald as possible. However, in this case as shown in figure 4 and 5 the current flow through the channel of M3 or M4 from antenna to gnd are not going through

the load or can be treated totally wasted by rds from another point of view. And the power consumption is directly proportional to the MOS capacitances. That's the reason why we decrease the MOS size will help the PCE. We still could not explain why this is not happened in heavy load condition by now.

After some more analysis and simulation, we find out that the actual wasted power of M3 or M4 at different load are very close. The total power consumption of different load varies significantly; and the wasted power at heavy load is actually becoming "un-noticeable". The graph below shows average power consumption of M3 at different loads. Besides the MOS size, the power consumption is proportional to the input voltage level.



In summary, the power consumption of the NMOS normal bridge rectifier can be divided into three parts:

- (1) The power consumed by rds of M1 and M2 while charging the vdd node and this power consumption cannot be eliminated. The way to improve is increase the gds of M1 and M2.
- (2) The power consumed by load resistor.
- (3) The power consumed by rds and MOS diodes Dbs of M3 and M4 as well as MOS diodes Dbd of M1 and M3 (actually, the value of Dbs and Dbd are identical in normal structure). The ways to improve is increase gds and decrease the MOS diodes. The two approaches are contradictory. Fortunately, the turn on voltage of the MOS transistor is lower than the diode forward bias voltage from our simulation. So the total power consumption is the sum of the load resistor and four MOS channel resistors. However, since we haven't taken the resistance of MOS capacitance into account, we should not make the transistor size too big in real design. When you do real circuit design, you should extract a suitable resistance value and add into the simulation. Then fine-tune the circuit size to achieve the best performance.

The power consumption of the NMOS gate cross-connected bridge rectifier can be divided into four portions:

- (1), (2), and (3) are same as the normal case.
- (4) The power consumed by r_{ds} when the voltages of two antenna nodes are above gnd. The way to improve is to decrease the r_{ds} , which is contradictory to the other power consumption optimization. Since the power consumption is proportional to the input level as well as the capacitance (MOS diode size), we can optimize the PCE by decrease the MOS capacitances.

Another issue we have to point out is that the above analysis does not include the power consumption of the MOS capacitors. The situation of the reality is even worse because of the Quality factor (Q) of the MOS capacitance. The MOS capacitors, like C_{bs} , C_{gs} , C_{gb} , C_{gd} , etc., all have serial resistance. The resistance of capacitors not only consumes more power, but also regulates the frequency up limit of the rectifier structure. It is always correct to increase the Q factor of the MOS capacitance so as to increase the PCE and the high frequency performance. Actually, the capacitance is usually determined by processes for given MOS transistor sizes. The best way to improve this is balancing the gds and the capacitance by careful analysis and carefully laying out the rectifier circuits. The first three questions we arouse in last section have been solved to some extent till now. The reader can choose the appropriate rectifier structures according to their own specific needs for the first step. Then keep what we have presented in mind to fine-tune the circuit to meet its optimal.

(1.4) PCE of NMOS charge pump circuit

Compared to the other rectifier structure, the NMOS charge pump is different and unique. Because of its lowest input level performance, it is attractive and forces us to do more analysis on it. The most widely used charge pump or voltage multiplier structure in solid-state circuits is the Dickson Charge pump. The figure 6 is a four-stage Dickson charge pump.

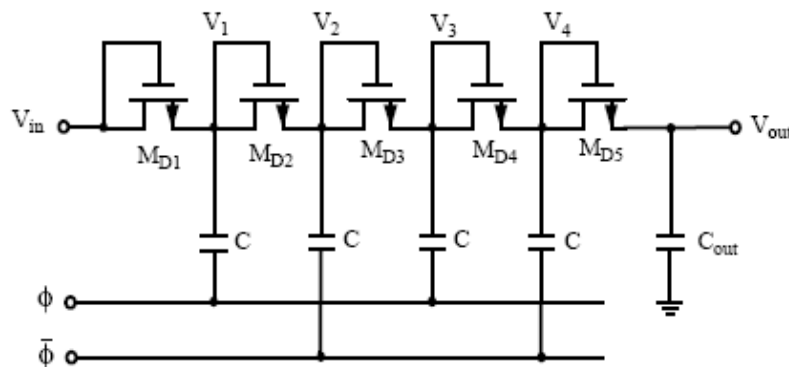


figure 6 4-stage Dickson charge pump

The output voltage of the diode-connected NMOS transistor Dickson charge pump is given by

$$V_{out} = V_{in} + N \cdot \left(\frac{C}{C + C_s} \cdot V_{\Phi} - V_m - \frac{I_{out}}{(C + C_s) \cdot f_{osc}} \right) - V_m \quad (\text{Equation 1.4.1})$$

The voltage fluctuation can be expressed as

$$\Delta V = \frac{C}{C + C_s} \cdot V_{\Phi} - \frac{I_{out}}{(C + C_s) \cdot f_{osc}} \quad (\text{Equation 1.4.2})$$

And the voltage gain of the charge pump can be expressed as

$$G_v = \Delta V - V_m \quad (\text{Equation 1.4.3})$$

As the clock voltage V_{Φ} level decreases, both the voltage fluctuation and the voltage gain will be reduced. Besides the effects of clock voltage level, the threshold voltage of the NMOS also affect the voltage gain. The equations above have not taken the bulk bias into consideration. Since the DC voltages of the NMOS source nodes will be above ground and all the substrates of NMOS transistors are connected to ground, the threshold voltage will be higher for every NMOS transistor than its forestage because of the substrate bias. Then the gain of the voltage will be reduced even more. The actual threshold voltage drop is around 1.0V for a CSM06 diode-connected NMOS transistor by our simulation. As for the output current, we have assumed two conditions in our first phase work. The first case is output power 50uW (at a reading distance of about 3.3m and the antenna gain of about 0 dB and 500-mW ERP, average input power to the tag is about 54uWⁱⁱ); the second is output power of 500uW. The output current for the first case at 2V is 25uA.

Figure 7 is the charge pump voltage multiplier we researched in our first phase.

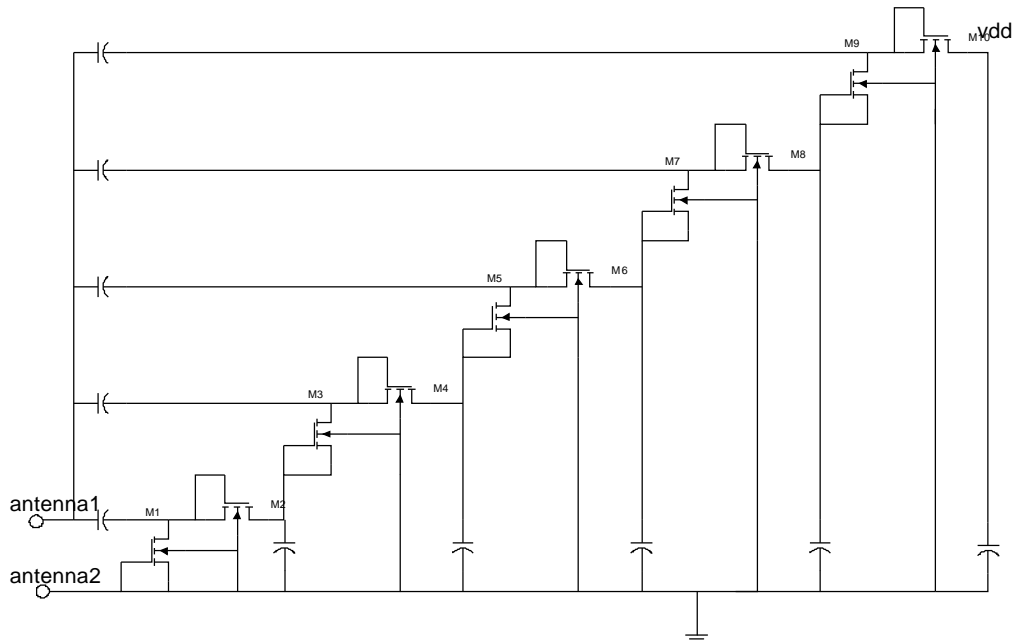


figure 7 charge pump voltage multiplier by diode-connect NMOS transistors

The voltage multiplier in our first phase research is actually more than five stages. If we treat the first two NMOS transistors and capacitors to be a voltage rectifier, then it is actually 8-stage Dickson charge pump. The difference is the clock signal feedin scheme.

The original Dickson charge pump uses non-overlap clocks to drive the consecutive stages. The charge pump voltage multiplier for the RFID tag uses the negative and positive input RF signal to drive the consecutive stages. Although the signal implementations are different, the equations still work for our structures. However, the clock signal for RFID is sinusoidal rather than the square wave of normal Dickson charge pump. So the threshold voltage drop would be even more if we considering the limited time to charge the current for load consumption. The figure 8 shows the simulation result of the voltage drop on M2 with different output loads. The minimum voltage drop is around 1.3 volt and the maximum voltage drop reaches 1.7 volt. The figure 9 shows the simulation result of the voltage drop on M2 without output load at different input signals. The input signal swings (Voltage peak to peak = 2 Volt) are the same, while the frequencies and wave shapes are different. One is 100MHz sinusoidal, one is 900MHz sinusoidal and another is 100MHz square wave with duty cycle of 50%. The minimum voltage drop, which is achieved by square wave is around 1.15V; the 100MHz sinusoidal voltage drop is nearly 1.2V; and 900MHz sinusoidal has a voltage drop of 1.3V

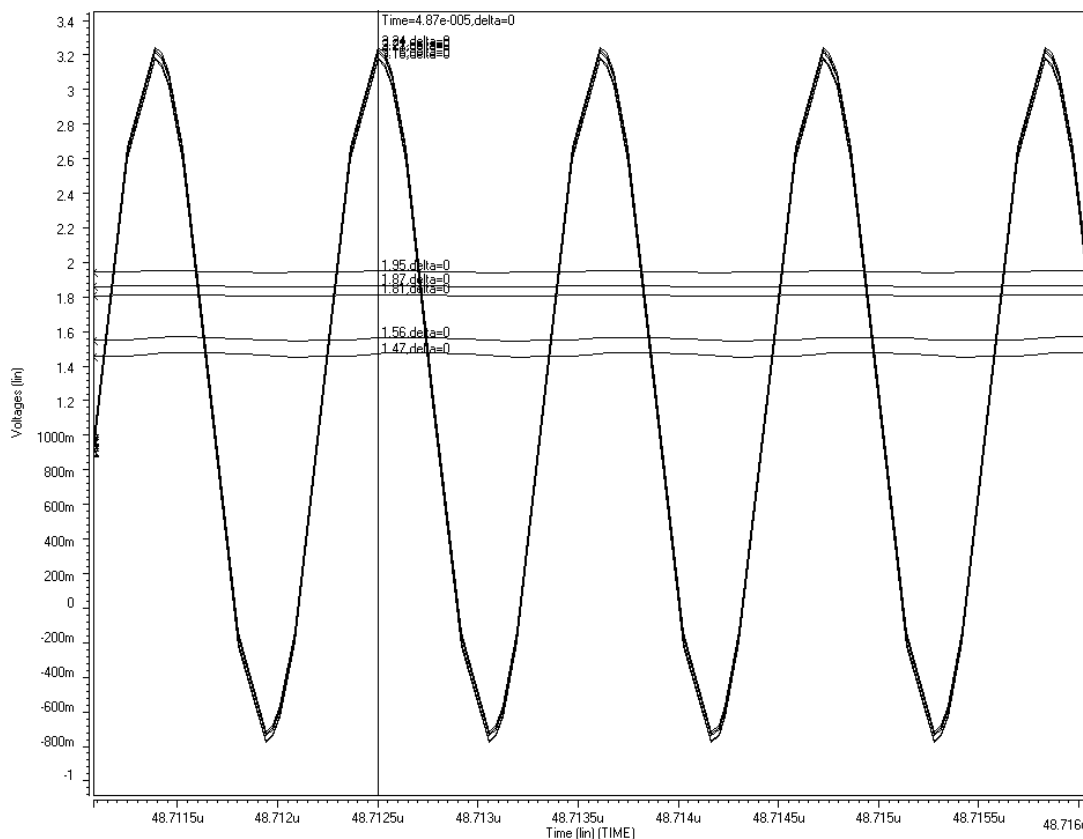


figure 8 Voltage drop on M2 at different output loads

Although we can achieve high voltage by stacking the charge pump stages, it is usually not applicable because of the stray capacitance in the integrated circuits and the power consumption overhead. We have learned that the power consumption of the charge pump voltage multiplier is about 5 times of the structure with best PCE index from our first phase research report. And the higher input level, the better PCE. This is exactly same as the NMOS bridge rectifier. The reason for this is the high channel resistance at

sub-threshold or around threshold. The problem is inherent to all the rectifier structures. So it is always right to resonant the input to a high voltage level to boost the PCE no matter the structure of normal bridge rectifier and the voltage multiplier.

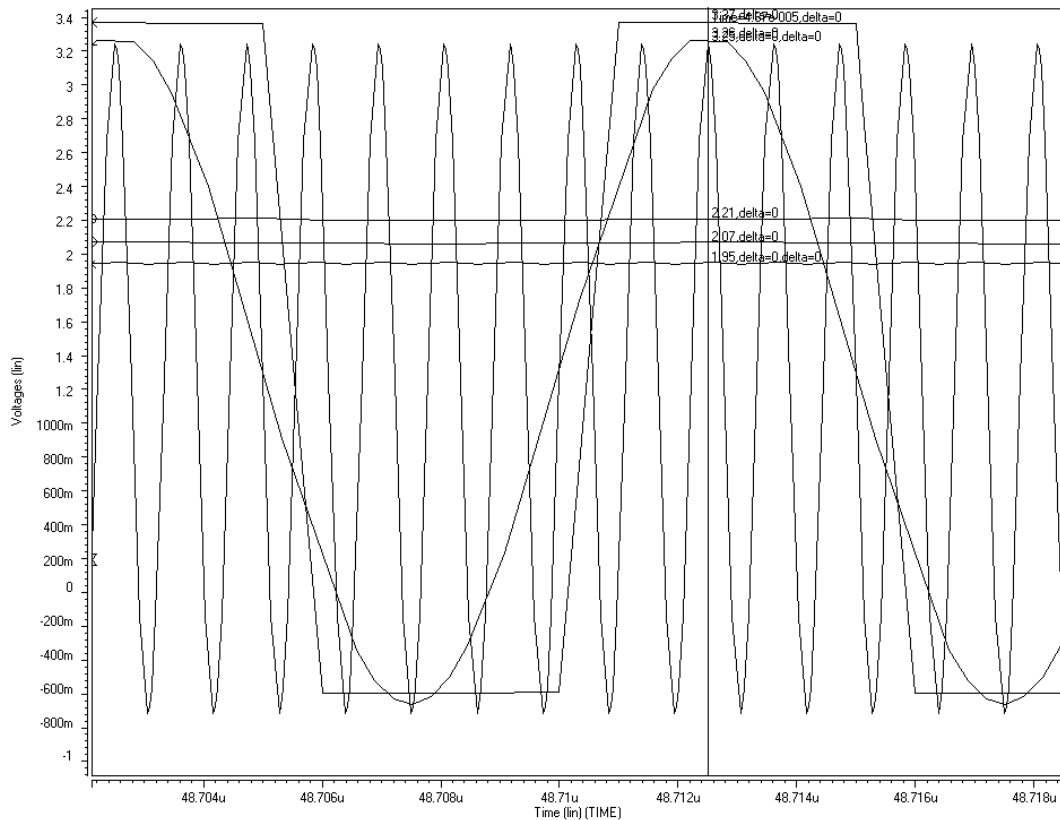


figure 9 Voltage drop on M2 at different input signals

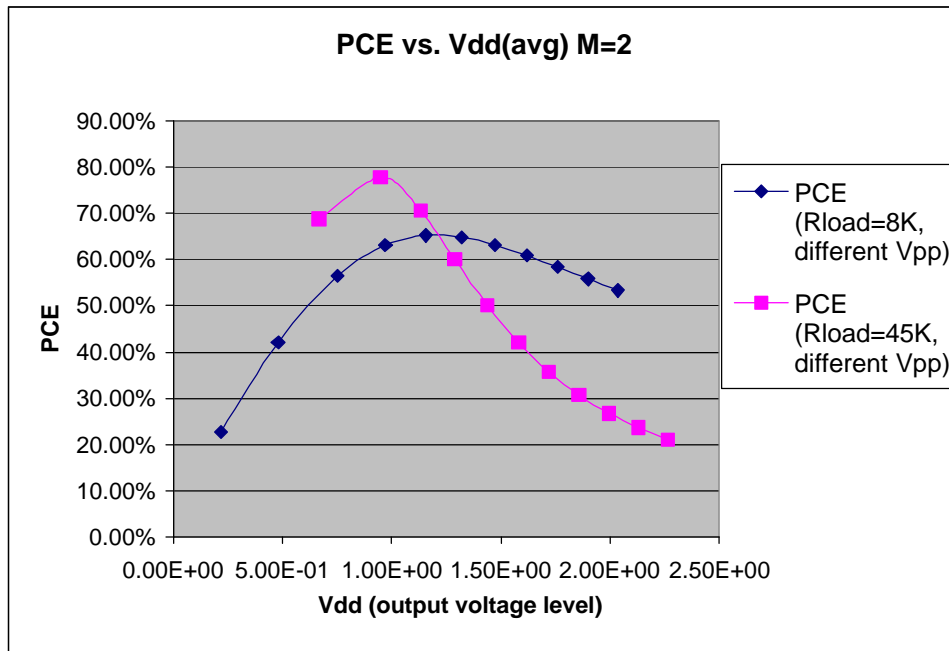
It is also obvious that all the output current have to be transferred by the NMOS transistors stage by stage to the high output voltage level. All the NMOS transistors will waste a part of the power that is fed into them. The more stages incorporated, the worse the PCE. From the PCE point of view, we should not use charge pump rectifier structure or use as little stage as possible. If the rectifier output voltage can meet the need with input RF signal level, we should use traditional structures for better PCE performance. However, if the input voltage level is too low to generate the preferred output voltage level, we have to use the voltage multiplier. Another application for charge pump is the RFID non-volatile memory. There are programmable non-volatile memories in those read-writable RFID chip and on-chip charge pump voltage multiplier usually generates the high programming voltage. It is necessary to incorporate the charge pump in such cases.

For a given output current, NMOS threshold voltage and charge pump capacitor, the voltage gain of the charge pump is determined by the equation 1.4.1. Although there are some alternative ways to improve the charge pump gain by modified cell formsⁱⁱⁱ, it is not applicable to make the structures work nicely at the UHF frequency range. As for the original form, we should make the threshold voltage as little as possible. The way besides the migration to better processes is to replace the NMOS transistors with low turn-on voltage integrated diodes. For example, the Schottky diode.

(1.5) PCE of NMOS and PMOS gate cross-connected bridge rectifier

We have found that the NMOS and PMOS gate cross-connected bridge rectifier can achieve over-all good PCE performance in our first phase research. It seems to be contradictory to the analysis we made in section 1.3. How can the NMOS and PMOS gate cross-connected bridge rectifier free from the penalty of the MOS switch characteristics?

As we known, this kind of rectifier structure can generate highest output voltage (excluding the voltage multiplier). The maximum output voltage for a 3V peak-to-peak input level would be around 2 to 2.2V. And another issue is that we have decreased the MOS transistor size to multiple equals 2 rather than 10 because of the leakage. So we varied the input voltage level to check the PCE and input level (output level) relationship. After a series simulation, we are able to plot out the relationship between PCE and output voltage, which is showed in the graph below.



We can see that the PCEs do have a peak value at a certain output level. The PCE will not remain high for high output voltage (in fact, the high input swing). This is the penalty of using MOS transistor as switch, just like we have analyzed in section 1.3. The turn-on time of the MOS transistors would be increased with the input level. And so does the counter direction waste current. The reason why the PCE drops less for heavier load is that the absolute value of the switch waste power consumption is proportional to the input and output level and thus the portion of total power consumption is smaller for heavier load. For the input value less than the peak point, we enjoyed the benefits of the low turn-on voltage. For the input value higher than the peak point, the waste currents begin to climb up and deteriorate the PCE. So we'd like to use the structure with

comparatively low input voltage levels. For example, for the CSM06 process, the PCE optimal value would be around 1.0V to 1.5V output and 1.5V to 2V input levels.

Summary of the causes of PCE differences:

We would be able to figure out the causes of PCE differences after all the above analysis. The readers are recommended to keep all the causes and suggestions as reference when you design your own RFID rectifier circuits. There would probably be some differences for different device models and simulation environments.

- (1) A large portion of the energy is consumed by the MOS transistor channel resistance. The channel resistance is higher at sub-threshold or around threshold voltage. The input level always helps the PCE for the diode-connected MOS transistor rectifiers. So the resonant at the input is crucial to the total quality of the rectifier as well as the whole RFID performance.
- (2) Without considering the capacitance and its Q, it is always better to have big MOS transistors because of the low resistance. The low resistance will boost the output voltage as well as the PCE. However, we could not afford too big MOS transistors in reality because of the capacitance and the quality factor of the capacitance. You have to use a more precise device model or extract the capacitance parameters from the layout to do post layout simulation before you finalize the design. Check and balance the MOS transistor size to get optimal performance.
- (3) The cross-connected gate rectifier structures bear an overhead of the switch operation of the MOS transistors. The structures only have better PCE at lower input levels. There would be waste power consumption for large input levels.
- (4) The PMOS transistor structures would have better output voltage level because of the less substrate bias effects. However, the conductivity of PMOS channel is usually smaller than the NMOS transistors.
- (5) Since every device in the circuits will consume power, it is easy to understand that the more transistors in the rectifier, the lower the PCE. However, it is necessary to use voltage multiplier in some cases. You should choose whether to use or not according to the input level as well as minimum available input power.

(2) Dipole antenna model

We have not taken the antenna and the impedance matching circuits into consideration till now. As we known, the antenna model and impedance matching circuits will add more constrains to our rectifier circuits. Our analysis will be more effective for the RFID application if we taken these two elements into our work.

We start from a dipole antenna model. Although dipole and monopole antennas are not necessarily the best candidates for UWB antennas, they are easy to manufacture and low cost.^{iv}

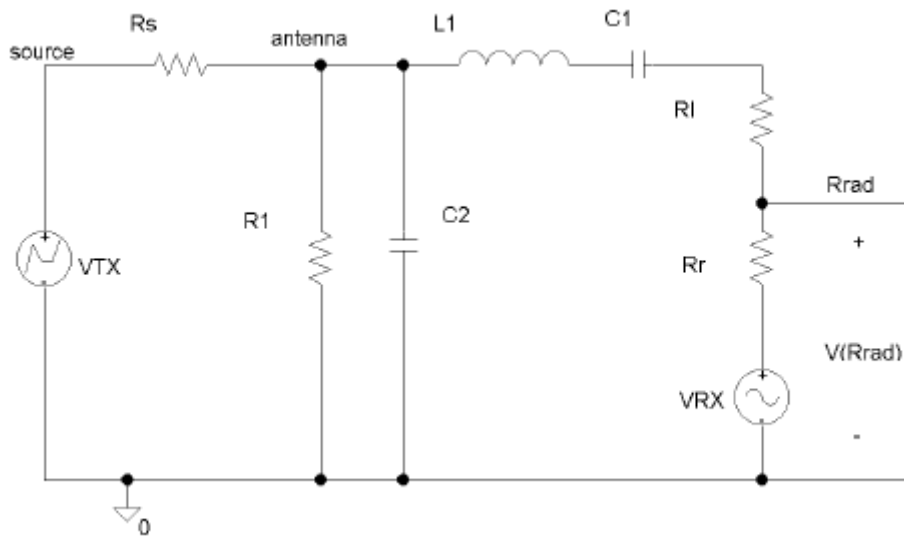


Figure 10 Electrical equivalent of a half wavelength dipole antenna connected to a 50 ohm source. The figure 10 is the electrical equivalent of half wavelength dipole antenna presented in ^{iv}. The Voltage source Vtx and Rs representing the output signals. The Rl stands for the antenna loss resistance, the Rr is the radiation resistance of the antenna. The Rl, which is 1Meg ohm, is used for Spice convergence. The C2 is used to improve the performance of the antenna above resonant frequency f0. Since the antenna is a linear network, we can use a voltage source for Vrx to simulate the antenna receive.

$$Z_a = \frac{V}{I} = (R_r + R_l) \cdot \left(1 + j\omega \frac{L}{R_r + R_l} - j \frac{1}{\omega(R_r + R_l)C}\right) \quad (\text{Equation 2.1})$$

$$f_0 = \frac{\omega_0}{2\pi} = \frac{1}{2\pi \sqrt{LC}} \quad (\text{Equation 2.2})$$

$$Q = \frac{\omega_0 L}{R_r + R_l} = \frac{1}{R_r + R_l} \sqrt{\frac{L}{C}} \quad (\text{Equation 2.3})$$

Since we want the RFID to work in the UHF region around 900MHz, we re-modeled the L1 and C1 to move the resonant frequency from 1.25GHz in ^{iv} to 900MHz. At the same time, we don't include the loss resistance and C2 at this time. The parameters of the antenna model are (we assume the Q=5):

L1=64.55nH

C1=484.5fF

Rr=73ohm

Rl=0ohm

Because the antenna is a linear system, we can use the same model for transmission and receive simulation.

(2.1) Single Schottky diode rectifier equivalent

If we use the simplest half wave rectifier structure built with Schottky diode, we will find that the Schottky diode is the deterministic factor of the input impedance because of the high value reservoir capacitor. We have got some reference values from our past discrete device analysis. If we use serial model like shown in the figure 11. Typically, the X_s impedance is capacitive and comes from a capacitance of around 1pF. At the frequency of 915MHz, the impedance can be computed to be $-j200\Omega$. In the series equivalent circuit shown above, R_s could be around 10Ω . This gives the total input impedance of the RFID chip as $10\Omega - j200\Omega$.^v

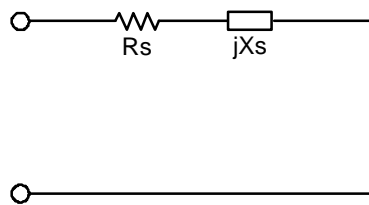


Figure 11 the equivalent circuit of the RFID circuit

We can learn that if we fully match the input reactance of the equivalent circuit, we still can only get as much as $\frac{10 \cdot 73}{(73 + 10)^2} \approx 10.6\%$ of the maximum power that the tag can receive.

In order to analyze the effect of load resistance and reservoir capacitor, we build a more detailed equivalent circuit of the RFID. The equivalent circuit includes the Schottky diode at work state and load resistor and reservoir capacitor as shown in figure 12.

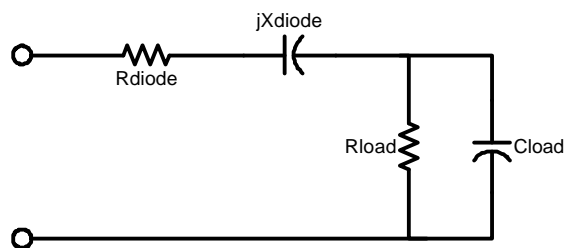


Figure 12 the equivalent circuit of RFID tag incorporating load and reservoir capacitor

If we convert the parallel connection of R_{load} and C_{load} to serial connection, the equivalent circuit is identical to the one shown in figure 11. The $R_s = R_{diode} + R_{serial}$; $X_s = X_{diode} + X_{serial}$.

For $R_{diode} = 10\text{ohm}$, $C_{diode} = 0.89\text{pF}$, and the X_{diode} at 900MHz is -199ohm .

And if we assume the $R_{load} = 8\text{K}$ and $C_{load} = 50\text{pF}$.

Then:

$$X_{load} = -\frac{1}{2\text{pf}C_{load}} = -\frac{1}{2 \cdot \text{p} \cdot 900\text{MHz} \cdot 50\text{pF}} = -3.54\Omega$$

$$R_{serial} = \frac{R_{load} \cdot X_{load}^2}{R_{load}^2 + X_{load}^2} = 0.00156\Omega$$

$$X_{serial} = \frac{R_{load}^2 \cdot X_{load}}{R_{load}^2 + X_{load}^2} = -3.54\Omega$$

$$R_s = R_{diode} + R_{serial} \approx R_{diode} = 10\Omega$$

$$X_s = X_{diode} + X_{serial} \approx X_{diode} = -199\Omega$$

We can see that because of the reservoir capacitance, the load has no much effects on the RFID tag input impedance.

If we decrease the Rload so as the Cload, Assuming Rload=45K and Cload=10pF.

Then:

$$R_{serial} = \frac{R_{load} \cdot X_{load}^2}{R_{load}^2 + X_{load}^2} = 0.00695\Omega$$

$$X_{serial} = \frac{R_{load}^2 \cdot X_{load}}{R_{load}^2 + X_{load}^2} = -17.7\Omega$$

$$R_s = R_{diode} + R_{serial} \approx R_{diode} = 10\Omega$$

$$X_s = X_{diode} + X_{serial} = -216\Omega$$

As the reservoir capacitor comes close to the diode capacitance, the load effect becomes more noticeable. However, since the reservoir capacitor is inversely proportional to the load resistance. The real part of the tag input impedance is determined by Schottky diode resistance. For the case that the reservoir capacitor is 10 times the diode capacitance, we still can say that the input impedance is determined by the Schottky diode.

(2.2) Resonant circuit issues

We can learn that the input voltage level always helps the PCE from the summary of PCE causes. So we may easily think of using the resonant circuits to boost up the input voltage level. However, there are more issues than we may thought at our first glance.

We have to use a kind of antenna to coupling the RF field anyway. And because of the receive bandwidth, the antenna Q should not exceed 9 to get a 100MHz bandwidth in 900MHz UHF system. If you use a dipole antenna like the one we presented in this document, the Q is around 4 to 5. At the resonant frequency, the reactance part of the antenna is omitted. For maximum power transfer, the resistive load should be same as

the antenna radiation resistor. For half wave dipole antenna, the radiation resistor is 73 ohms.

With the antenna gain about 0dB and 500-mW ERP, the input power at 2m is about 150-uW. We can calculate out the V_{rx} value of figure10 (peak-to-peak) by short-connect the node 'antenna' in figure 10 to ground.

$$V_{rx(p-p)} = 2\sqrt{2} \cdot \sqrt{P \cdot R_r} = 2\sqrt{2} \cdot \sqrt{150\mu W \cdot 73} = 0.296V$$

For a 50 ohms resistive load, the input voltage (peak-to-peak value) on load is:

$$V_{load(p-p)} = 2\sqrt{2} \cdot \sqrt{P \cdot R_r} \cdot \frac{R_{load}}{R_{load} + R_r} = 2\sqrt{2} \cdot \sqrt{150\mu W \cdot 73} \cdot \frac{50}{73 + 50} = 0.120V$$

For a fully matched resistive load (73Ω), the peak-to-peak voltage will be no more than 0.15V. If the load resistive is smaller than 73 ohm, the peak-to-peak voltage will be less than 0.15V. While the load resistive is larger than 73 ohm, although the peak-to-peak voltage on load will goes up than 0.15V (but less than 0.3V), the output current will decrease so as to the output power.

So for maximum power transfer, we'd like to make the load equals to the antenna radiation resistor. For the input voltage level, we'd like to make the load as large as possible. However, considering the maximum power that tag is able to get, the maximum peak-to-peak voltage on the load will never exceed the value given by:

$$V_{rx(p-p)} = 2\sqrt{2} \cdot \sqrt{P \cdot R_r} \quad (\text{Equation 2.2.1})$$

$$V_{load(p-p)} = 2\sqrt{2} \cdot \sqrt{P \cdot R_r} \cdot \frac{R_{load}}{R_r + R_{load}} \quad (\text{Equation 2.2.2})$$

For instance, we have calculated maximum peak-to-peak voltage on load will be **0.296V** for 150uW input power and 73ohm radiation resistor. Because the input power is physically determined, the only way to increase the voltage on resistive load is to increase the radiation resistor and make the load resistor value as large as possible. There is no use for resonant circuit to boost up the peak-to-peak voltage on the pure resistive load.

However, the input impedance of a real tag chip usually has resistance and reactance. Like the single Schottky diode rectifier in last section, whose impedance is 10Ω – j200Ω. With the reactance, we would be able to add resonant network (usually impedance matching network at the same time) to boost up the voltage across the tag.

If we use the antenna at its self-resonant frequency, the resonant/matching network and the tag chip will form a new resonant circuit. In order to match the tag chip input impedance, the Q of this new resonant circuit is actually determined by:

$$Q = \frac{X_s}{R_s}$$

The X_s is the serially configured reactance of the tag chip while the R_s is the serially configured resistance of the tag. The maximum Q will be 20 for the impedance of $10\Omega - j200\Omega$. The quality factor of the resonant/matching network will even decrease the Q . We may figure out the maximum voltage across the tag chip like:

$$V_{p-p} = 2 \cdot \sqrt{2} \cdot \sqrt{P \cdot R_r} \cdot \frac{R_s}{R_r + R_s} \cdot Q \quad (\text{Equation 2.2.3})$$

For the impedance of $10\Omega - j200\Omega$, the Q equals 20. And the peak-to-peak input voltage on the tag chip will be **0.7V** (the other conditions remain the same as the preceding analysis). Under such a low input voltage level, no other rectifier structure will work except voltage multiplier circuit with low forward bias voltage diode.

If we analyze the equation 2.2.2 and 2.2.3 more, we can find that the maximum peak-to-peak voltage for a given tag chip input resistance could be reached when antenna radiation resistance equals the tag chip input resistance ($R_r = R_s$). And the value is proportional to the square root of the tag chip input resistance.

We may expect the input impedance to be different from the one that we have analyzed. However, the input capacitance has some limitation in reality. Considering the input frequency is 900MHz, the reactance caused by input capacitance of 1pf can be -176.8Ω . It is hard to decrease the input capacitance in reality, so if we try to increase the input resistance so as to increase the input voltage level, the quality factor will decrease which in turn will decrease the input voltage level. Actually, the impedance of the tags are within the same order of the one, which we have analyzed in reality. That means the input voltage level that we can expect is around the magnitude of 1V for 150uW input power even if we have added some ideal resonant circuits. This pushes us to incorporate the voltage multiplier structure with low forward bias voltage diode.

(3) Schottky diode voltage multiplier

Given the reality that we could only get an input voltage level at the magnitude of 1~2V at low input power level, we would not be able to use the traditional bridge rectifier in UHF RFID tag. The typical working voltage is 2.5V to 3V for 035um CMOS process and normal working voltage cannot be lower than 1.5V for 0.18um CMOS process. We would not be able to use gate cross-connected PMOS and NMOS complimentary bridge rectifier under such low input level either. If we suppose that the threshold voltage goes down with the feature size, we may probably be able to use the MOS switch operation rectifier in more advanced processes. However, we are still not able to get high Power Transfer Efficiency under low input voltage levels because of the large channel resistance around the threshold voltage (please refer to the PCE cause analysis section in this report). So if we want to make the tag chip rectifier have better PCE performance, we have to use Schottky diode although most of the CMOS processes don't support the Schottky diode.

Before we would be able to build any Schottky diode models from a standard CMOS process, we use a discrete Schottky diode model to evaluate the efficiency.

We choose discrete Schottky diode with low turn-on voltage and small Cd from Philips Semiconductor. The device is 1PS79SB63. The maximum forward bias voltage is 200mV at forward current of 0.1mA and the maximum diode capacitance is 0.5pf.^{vi}

We substitute the NMOS with 1PS79SB63 Schottky diode of figure 7 and re-do the simulations. And the simulation results are (not including the antenna model):

<i>Conditions (load, cap, input Vp-p)</i>	<i>Output DC voltage (V)</i>	<i>Pout (W)</i>	<i>Ptotal (W)</i>	<i>PCE</i>
8K, 100pf, 0.5V	2.16	5.829E-4	1.437E-3	40.6%
8K, 100pf, 1.0V	6.044	4.5668E-4	7.7993E-3	58.6%
8K, 100pf, 1.5V	9.9948	1.248E-2	1.901E-2	65.6%
45K, 20pf, 0.5V	2.6	1.5037E-4	3.689E-4	40.8%
45K, 20pf, 1.0V	6.77	1.0185E-3	1.6902E-3	60.3%
45K, 20pf, 1.5V	11.12	2.7486E-3	4.0758E-3	67.4%
100K, 20pf, 0.5V	2.8317	8.0184E-5	2.246E-4	35.7%
100K, 20pf, 1.0V	7.0999	5.0409E-4	9.5916E-4	52.6%
100K, 20pf, 1.5V	11.56	1.3364E-3	2.2175E-3	60.3%

We manage to supply an output current around 30uA at 2.8V output DC level with 0.5V peak-to-peak input level. And the PCE is much better compared to all the other rectifier structures we have analyzed. The simulation results are very promising. However, the problem is that most of the standard CMOS processes do not support the Schottky diode. We have to modify the processes so as to incorporate the Schottky diodes. Some of the works are already been done.^{vii} The results are optimistic.

(4) Summary

In our second phase research, we have analyzed the PCE causes of different rectifier structures. And we find that the input level affects the PCE of rectifier structures. Although we may get higher output voltage by making the MOS transistors working as switch, there is a power penalty at high input level because of the counter-direction current.

Considering the antenna model, the maximum available input power and the input impedance of the tag chip, we would be able to feed in a tag with around 1V peak-to-peak voltage. With such a low input voltage, only the voltage multiplier with Schottky diode would have a reasonable good PCE performance as well as the output DC voltage.

In future, more work will be done on the Schottky diode modeling and incorporating into standard CMOS processes.

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