Brief Comparison of Different rectifier structures for HF and UHF RFID (Phase I Draft version 1.0)

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Background

The contact-less smart card, the HF and UHF RFID all incorporate rectifier circuits to convert the coupled AC continuous (maybe un-continuous in some cases) electro-magnetic carrier waveforms to a DC voltage and serve a power supply for the rest part of the chip circuits. So rectifier is one of the essential parts of the RF interface circuits in the contact-less smart card or the RFID tag. This article compares different rectifier structures from the research work done for the past a few years and tries to present conclusion on their advantages and disadvantages, which we assume will be helpful for reader to choose their appropriate rectifier structures considering their own situations.

The major challenges of the RFID rectifier are:
(1) Ultra-low input power level which has not been thoroughly investigated or reported before;
(2) Alternative way to over come the “dead-zone” rather than Schottky diode; [i]
(3) Implementation of Schottky diode in low-cost digital CMOS process.

We will not exclude Schottky diode solutions in our research work. However, since Schottky diode isn’t compatible with current low-cost CMOS process, we will come to it later in phase II as a discrete section. At the same time, since the impedance matching between antenna, resonant circuits, impedance matching circuits and the rectifier circuits as well are crucial to the rectifier efficiency, they should be treated as a whole. However, in order to make an apple-to-apple comparison on the rectifier structures themselves, we do not include all these factors at this time. We will add them in phase II.

Simulation methods and environments

Before the comparison work, it is important to setup a correct simulation method and comparison standard. The most import performance index is the Power Conversion Efficiency (PCE) of the rectifier circuit, which we can define as the **Pout/Pin** of the rectifier circuit. Pout is the output DC power of the rectifier while the Pin is the input RF power.

In phase I, we do not incorporate the resonant circuits and the impedance matching network in our simulation. We just use a voltage source to feed in the RF power. On the output end, we use a passive resistor to represent the load. See figure 1 for a single diode simulation setup.

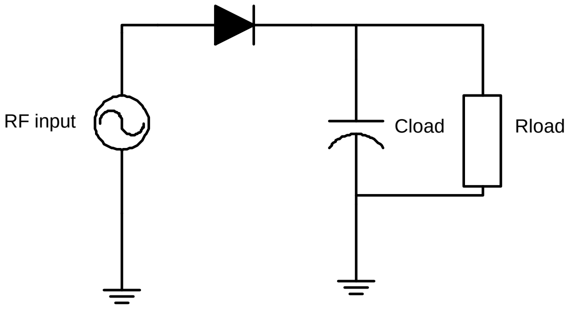


fig. 1

Because the input of the rectifier is an AC power source, the power issue is not as clear as the one in DC. Basically, there are three types of AC power: time averaged, maximum or minimum (peak), and instantaneous. The time averaged is the power that averaged by a period of time, which is usually used in the battery life estimation and junction temp calculation. The maximum and the minimum power are the peak values of the power in a period of time. The instantaneous power is the power of a definite time, or the power as a function of time. Another important measurement we always heard of is the “Root Mean Square (RMS)”. We usually use RMS value to measure the effective value of a voltage or current. If the RMS value of an AC waveform (voltage or current) is the same as a DC value, then the power dissipations on a resistive load are the same.

The tool we use to simulate is Star-Hspice (version 2000.2). Star-Hspice computes dissipated or stored power (instantaneous power) in each passive element (R, L, C), and source (V, I, G, E, F, and H) by multiplying the voltage across an element and its corresponding branch current. While for semiconductor devices, Star-Hspice calculates only the dissipated power. The power stored in the device junction or parasitic capacitances is excluded from the device power computation. Star-Hspice also computes the total power dissipated in the circuit, which is the sum of the power dissipated in the devices, resistors, independent current sources, and all the dependent sources. The total power dissipation is calculated by ‘measure’ statement with the variable ‘power’. The ‘measure’ statement has several measurement options to use, like average, RMS, min, max, etc. So the next problem would be which measurement to choose, RMS or average?

The RMS value is used to calculate the effective work done on a resistive load by a voltage or current source. For example, there is a sinusoidal wave with peak voltage Vp-p added to a resistive load. See figure 2.

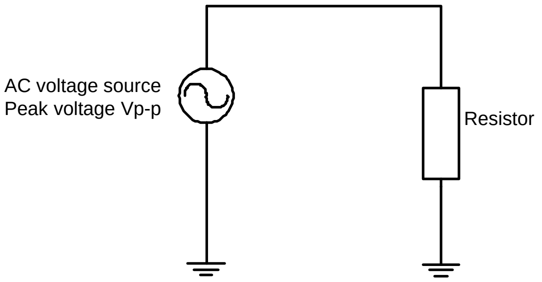


fig.2

How about the output power of this voltage source? As we know, the power dissipated on the resistor is the total power consumption of the circuit. And the resistive load dissipated power P(resistor)=V^2/R=I^2*R for a DC value. The value of V and I would be RMS value while it comes to the AC signal. For AC signals no matter what their frequencies, wave shapes are, if their RMS values are the same, the work efficiency or power consumption on the resistor load are the same. That's the way we use RMS value rather than average or peak value to evaluate an AC signal's working efficiency on a resistive load. So we usually use the RMS measurement to measure the voltage or current effective value. Since the power consumption on a resistive load is proportional to its RMS voltage or current, we may also find RMS power in some cases.

In Star-Hspice, the 'measure' statements report functions of the output variable rather than the analysis value. So it should be treated as mathematical rather than analysis in a more precise view. The variable 'power' of one element is given by multiplying the voltage across an element and its corresponding branch current.

$$P(t)=V(t)*I(t)$$

In order to get a correct calculation method, we did several experiments. For a resistive load, we use 'measure' statement to measure both the average and RMS value of the variable 'power' and get different results. At the same time, we measure the RMS value of the current as well as the voltage across the resister. We found that the power calculated by Irms^2*R or Vrms^2/R equals the one get from measure of the average value of 'power'. According to the basic work law of the resister, the measurement of average value of 'power' is the correct approach to the circuit power consumption. Actually, the variable 'power' itself is the product of V and I, the average of it is more sensible considering the circuit power dissipation. Another support comes from the law of energy conservation. If we add up all the average power consumed or stored in the circuit elements or sub-circuit, the value will be same as the sum-up of average power of the power sources with opposite polarity. It's not the case for RMS measurement of 'power' variable. That's why we cannot use the RMS measurement of power in Star-Hspice simulation.

If we dig deeper, let's take a look at the measurement (calculation) method of the RMS 'power'. For RMS calculation, it squares the value of variable 'power' for the first step, so every value will go positive before they are averaged. However, there could be positive or negative power for an element or sub-circuit for some periods of time during its operation. For example, there is a sub-circuit with power storage capacitor outside of it, like an EEPROM. The power from the sub-circuit may goes to negative to charge the power cap and then it goes to positive while the power capacitor re-charges the current back sometime later. If you calculate the RMS value for this sub-circuit power, you will take the in and out power twice. Actually this sub-circuit doesn't consume any power for the whole period of time. In fact, the Power Conversion Efficiency is the index of the power consumed or dissipated by the load resister compares to all the energy consumed by the resistive elements in the whole circuit. The higher the efficiency is, the higher portion of all the energy is used by the load. So we can use the Star-Hspice tool to calculate the PCE in this way: PCE= P(average value of load dissipation)/P(average value of total power dissipation). The total power dissipation variable of the whole circuit is named 'power' in Star-Hspice.

Besides the PCE, we have to make clear another concept. We have to remember the PCE and the output DC voltage level is not a same problem. Sometime, they vary in the same direction. For example, if we increase the load, both the PCE and DC voltage of the rectifier will drop. Sometime, they can vary in a different direction. For example, we can sacrifice the PCE for higher DC output voltage by using a charge pump structure rectifier.

Simulation work

We choose 7 different kinds of rectifier structures for comparison. They are:

(1) Single diode structure
(2) NMOS bridge rectifier structure
(3) NMOS with two MOS gate cross-connected bridge rectifier structure
(4) PMOS bridge rectifier structure
(5) PMOS with two MOS gate cross-connected bridge rectifier structure
(6) Gate cross-connected PMOS and NMOS bridge rectifier
(7) NMOS diode 5 stage charge pump rectifier

There are not many references on the power conversion efficiency simulation methods. So we are trying to build some suitable simulation methods for the rectifier PCE during our simulation work. We compare several aspects for every kind of rectifier structure. Firstly, we find out the minimum work input level, Vp-p(min); Secondly, we get the power conversion efficiency (PCE). Since the PCE varies with the input level, load level, output DC voltage level and many other conditions, the comparison of PCE without other conditions will be misleading. So we use several indexes to show the PCE. The indexes we use include: the PCE curve vs. total power consumption (various input level with fixed load and diode sizes), the PCE curve vs. load resistor (various load with fixed typical input level), the PCE curve vs. diode/MOS sizes (various diode/MOS sizes with fixed typical input level and load), the PCE at minimum input level, the PCE at normal operation input level. Considering the typical load, if we suppose the power consumption of the chip is 50uW and the output DC voltage 1.5V, and then the load will be around 45K ohm for simulation. If we suppose the power consumption of the chip is around 500uW and the output DC voltage is 2V, then the load will be around 8K ohm for simulation. We use these two load-resistors as typical loads.

Here we have to point out another important issue. Since we use an ideal voltage source as the input, the total power consumption is the sum of the output load power and rectifier power consumption. So the PCE would possibly higher than 50%. In reality, the received power can be modeled as voltage source with inner resistance and reactance. So the actually PCE of the whole RFID tag will never exceeds 50%. We should keep this in mind or we will find some simulation results to be misleading in this report.

(1) Single diode structure

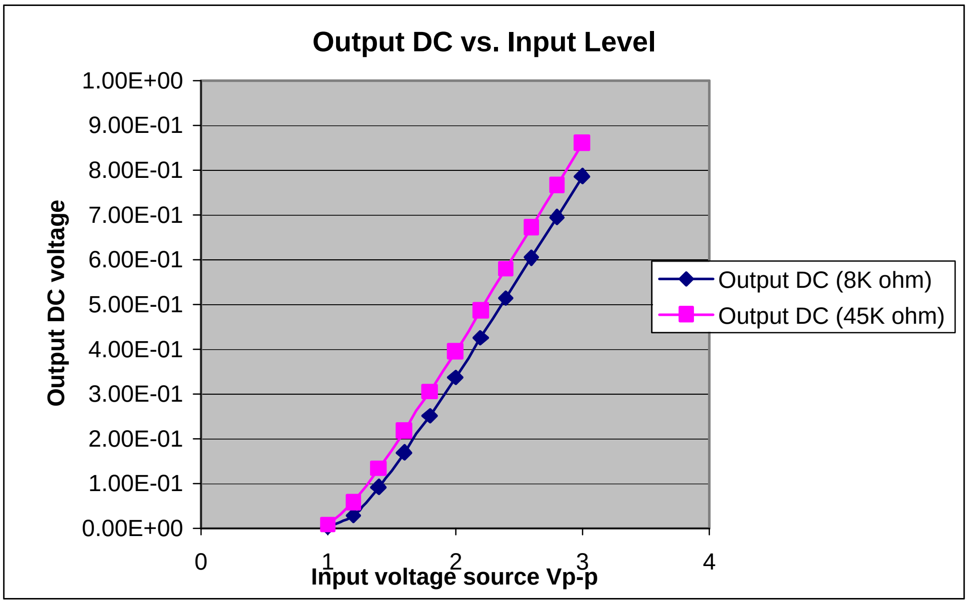
The single diode approach is the simplest one. The configuration is shown in figure 1. We use two different kinds of diode model presented by FAB. One is the Chartered Semiconductor CSM08 process. The other is the Chartered Semiconductor CSM06 process.

(1.1) CSM08 diode model

Firstly, we use CSM08 diode model for simulation. The reason we use CSM08 diode model for simulation is that the model is a near ideal junction diode model on a CMOS process. The model does not include the junction capacitance parameters. And the model parameters are extracted from a large junction area diode. The area is 45000e-12 square meters and the peripheral is 1180e-6 meter. If the junction is a rectangular, that means dimension of the junction will be around 450um*100um. It’s a huge junction diode. It should not be able to work at UHF frequency for rectifier in reality. However, since the junction capacitance parameter is not included in the model parameters, we can use this ideal model to get some basic insights.

(1.1.1) Minimum working input level

The minimum input level indicates the dead-zone of the rectifier. Since the single diode rectifier can only make use of half of the RF input source. So the minimum working input level is high. The diagram shows the output DC voltage vs. input level. The rectifier can only generate a DC output over 0.1V at 1.4V Vp-p or 0.7V single sided input level. The bigger the value of load resistor, the higher the output DC voltage.

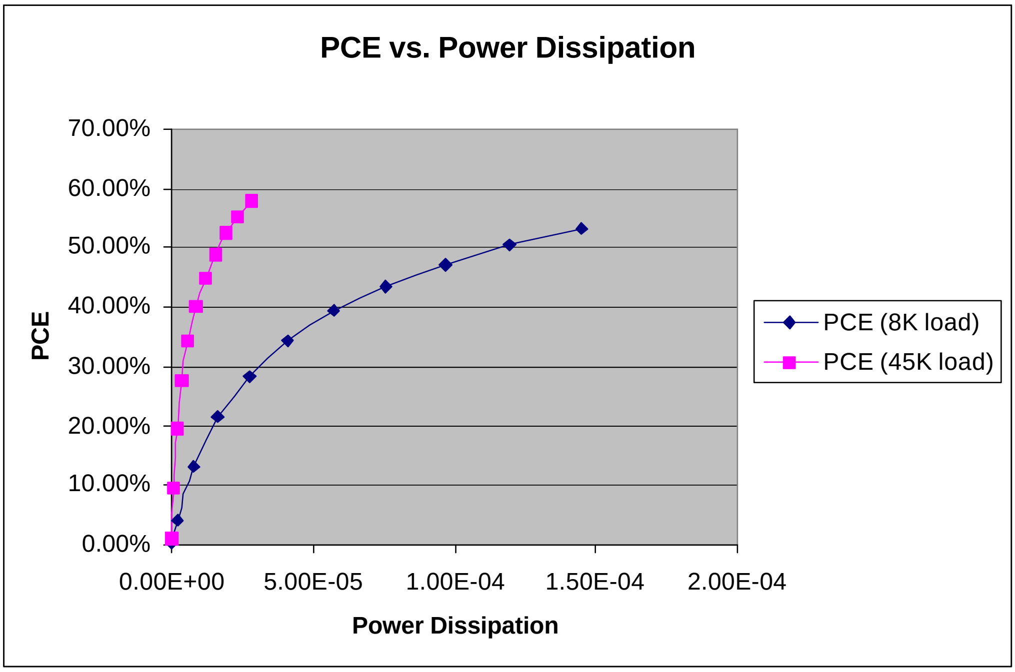


(1.1.2) Power Conversion Efficiency (PCE) vs. Input Power

The PCE of the rectifier is what we considering the most important to investigate. However, just like what we mentioned before, the PCE is varying with the other conditions. Since we use the Hspice measurement of total power dissipation of the circuit as the input power and the load resister power dissipation as the output power, the PCE for the single diode rectifier will be different from the real case. This is because the negative period of the voltage input will only draw a little leakage current and make the power dissipation of the negative period quite small. However, if we consider the real case, we will find that the negative half period power will be reflected back to the antenna, which means we waste the power of the whole negative half period. So the PCE divided by 2 or so will be more close to the real case for the single diode rectifier structure.

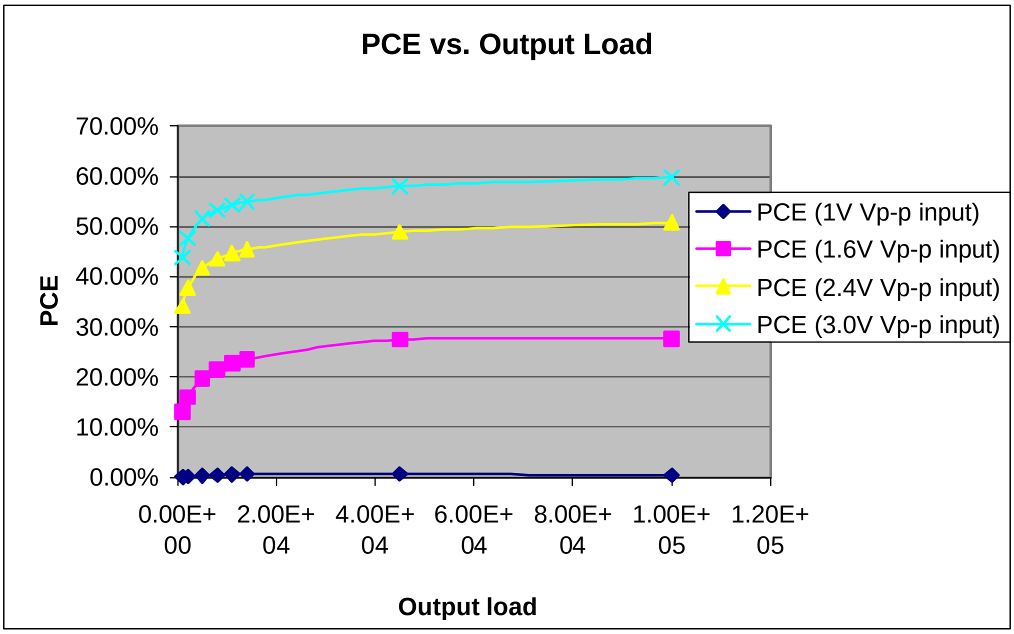
Since our major concern by now is the output power vs. total power dissipation by the rectifier itself and the load, we still use the PCE calculation method without modification.

We can see that the PCE goes up with the Power Dissipation (Input Voltage Level). Lower diode resistance at higher input voltage level causes the improvement. It is easy to learn the characteristic from the diode I-V curve. And the PCE will go down if the load becomes heavier. From this graph, we can see that if you want to remain high PCE at lower input level (or power), the only way is to decrease the load or the power dissipation of the whole chip circuit. That means to get a good work range of the tag, we have to not only design a power efficient rectifier, but also minimize the power consumption of the whole chip.



(1.1.3) Power Conversion Efficiency (PCE) vs. Load

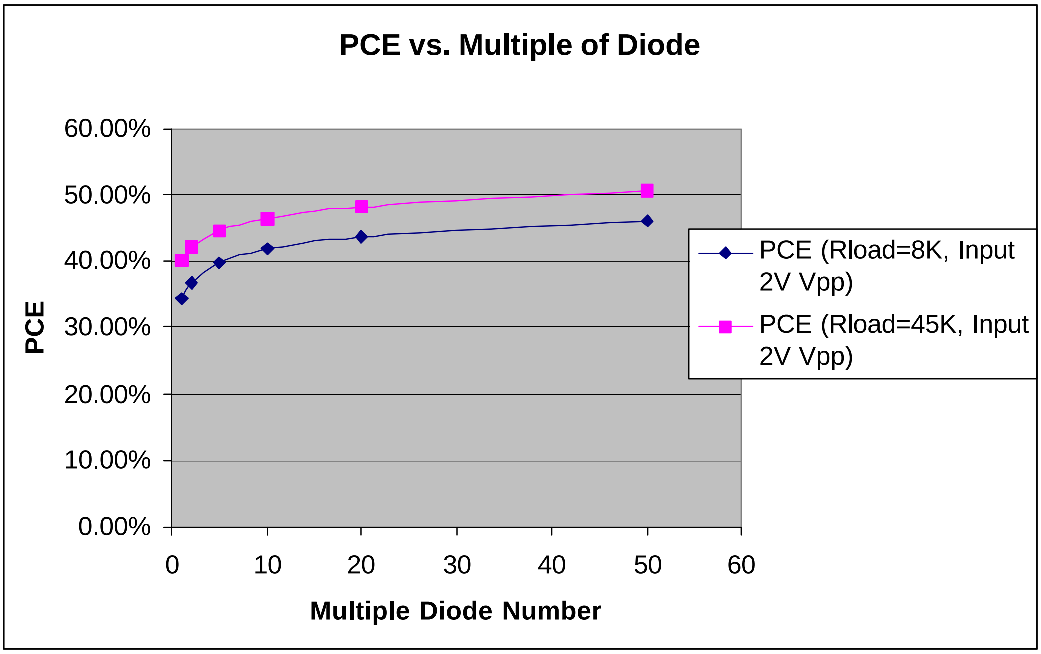
In order to make the relationship between PCE and load clearer, we did some more simulations on it. We compared the PCE versus load at different input voltage levels. All the curves show a trend that the heavier the load, the lower the PCE. Of course the high input voltage level will help the PCE like we have seen in last part. The PCE drops sharply while the load resistor becomes less than about 5K ohm.



(1.1.4) Power Conversion Efficiency (PCE) vs. Diode Size (multiple)

In fact, the diode we use to simulate is already too large to use. However, we still want to do some simulation on the PCE vs. diode size to see the trend. We use 2V peak to peak as a typical input. The diagram shows that the PCE goes higher with the diode size.

The reason is that the resister goes down with the diode size. It seems so fantastic. However, the truth is that the model does not include junction capacitance. If we taken junction capacitance into account, we will never get such optimal results. We will come to it when we use CSM06 diode model. Remember, the results from this diagram are just for reference.



(1.2) CSM06 diode model

The CSM06 diode model is extracted from two diode structures with different area to periphery ratio, as shown below (low voltage p+/nwell diode):

Area-dominant: A=4.6e-8, P=1.184e-3

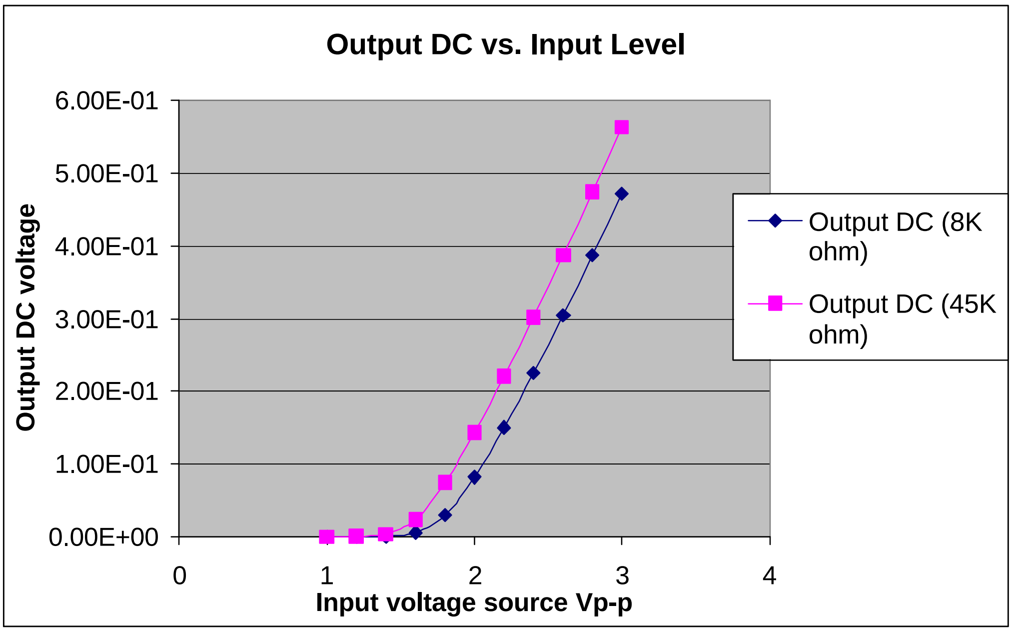
Peri-dominant: A=1.96e-8, P=2.80784e-2

If we choose area-dominant one, we will see that the junction size will be around 500um*92um. Then we go on with thejunction capacitance and ohmic resistance. The CJ0=7.355509E-4*4.6E-8=33.84pf. The RS=1.8E-6/4.6E-8=39.1ohm. We cannot use the diode for 900MHz operation because of the junction capacitance.

So we try to build a smaller size junction diode to do the simulation. We choose the size of 5um*5um. Let's calculate the junction cap: CJ=7.355509E-4*25E-12=0.018pf. And before we going on the simulation, we should modify some of the model parameters presented by the fab. The Rs value of the model is 1.8E-6/m^2 which is extracted from the diode structures we mentioned at the beginning of this section. However, if we do not change the Rs value for a small junction area, then the Rs value will be unreasonable. For instance, the Rs value of a 5um*5um junction area will be 1.8E-6/25E-12=72Kohm which is not applicable. Actually, the ohmic resistance of the diode is not very large. A good layout design will lead to 10 to 40 ohm totally. Since the model level is 3, we just modify the Rs value and maintain the total ohmic resistance of the 5um*5um diode to be 39.1ohm. All our simulation results are based on this modified and shrink diode model.

(1.2.1) Minimum working input level

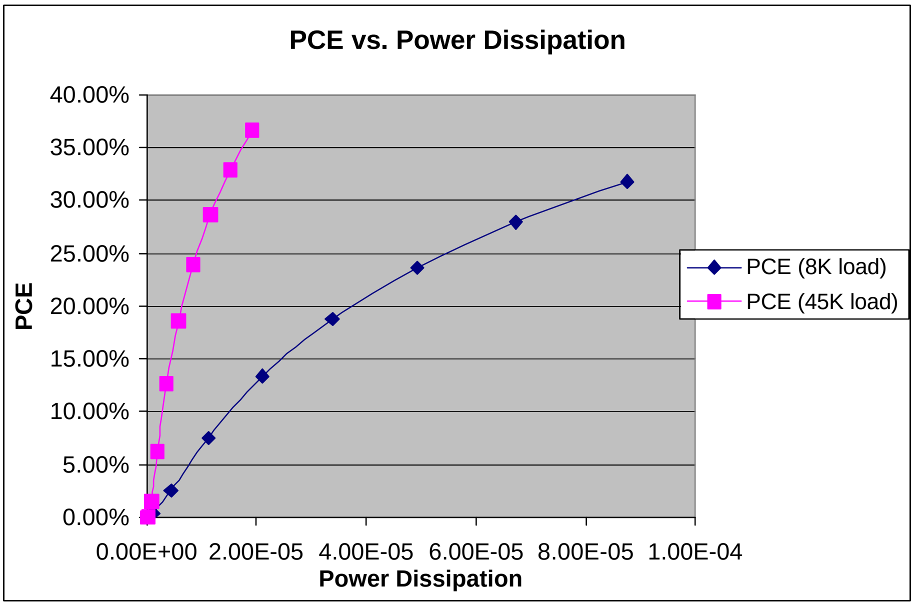
The minimum working input level is larger than that of the CSM08 diode model. The rectifier can only work for the input level larger than 0.9V single side.



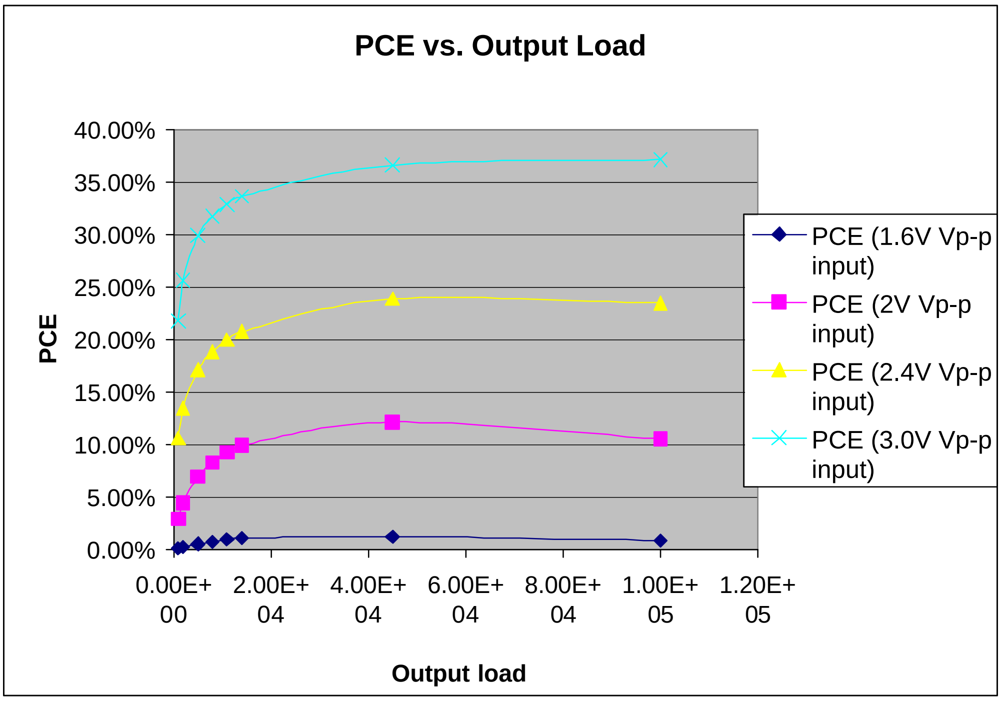
Same as the CSM08 diode model, the heavier the load, the lower the minimum working input level.

(1.2.2) Power Conversion Efficiency (PCE) vs. Input Power

Besides the output voltage levels are lower than CSM08 model at same input levels. The PCE is lower than the CSM08 model. The major reason for this is the existence of the junction capacitance. The impedance of junction capacitance at UHF frequency range is low enough to draw current from the output DC power storage capacitor during the negative half period.



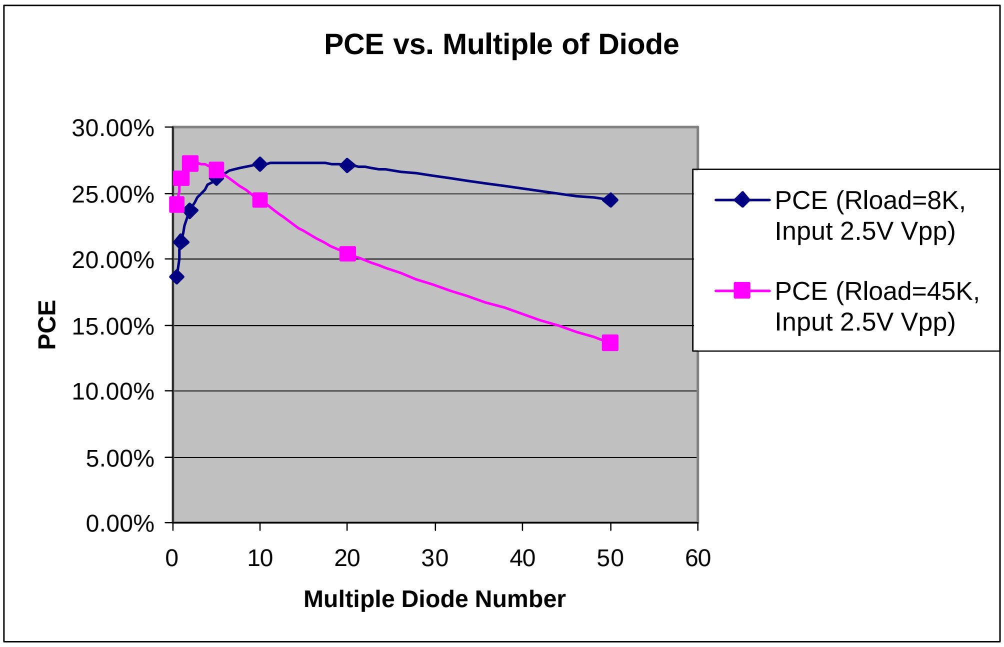
(1.2.3) Power Conversion Efficiency (PCE) vs. Load



We can see that the PCE go up with the output load resistor values. If we look carefully, we can find some exceptions on the graph. Some curves show a small drop at the load resistor of 100K ohm. What is the cause? After careful analysis of the simulation results, we found that the output supply voltage is still going up while we measure the PCE in the simulation. That means a part of the energy generated from the input voltage source is stored in reservoir capacitor and be treated as ‘waste’. If we exclude this part energy from the total power consumption, we would be able to get higher PCE. The reason for why the PCE at 3.0 volts input level does not have the drop is that the output supply voltage has already been boosted to its up limit while we take the measurements. The higher the input level, the faster the output voltage can be boosted to its upper limit. So we can say that the PCE versus output load relationship is still work: the heavier the load, the worse the PCE.

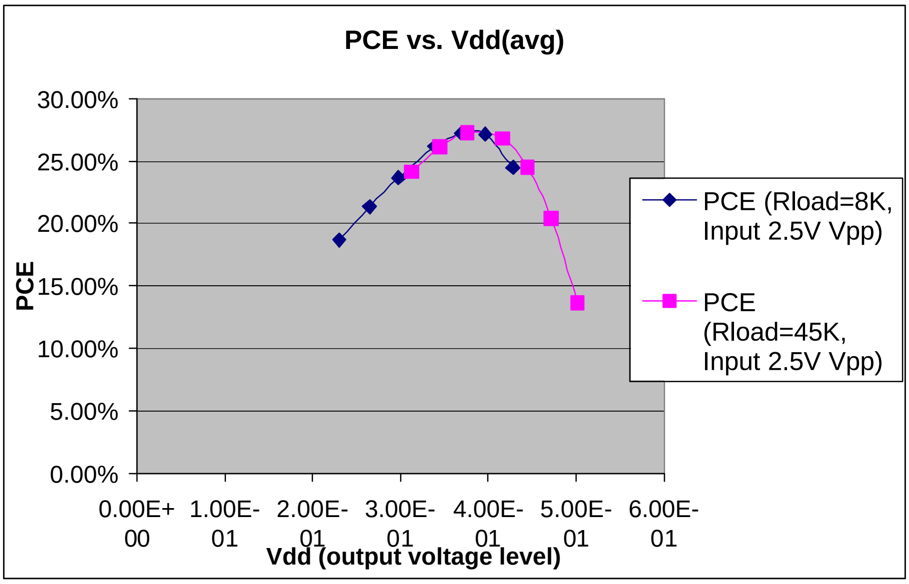
(1.2.4) Power Conversion Efficiency (PCE) vs. Diode Size (multiple)

Unlike the one of CSM08 model, the CSM06 model includes the junction capacitor parameters. So the PCE vs. diode size here will be more realistic than the last section.

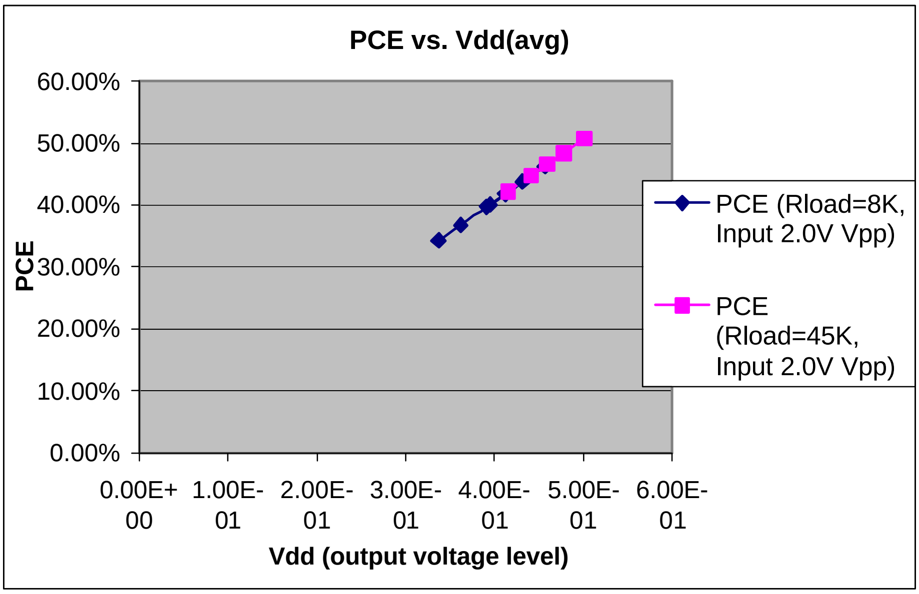


We can see that the PCE goes down sharply when the diode size goes up. The PCE can reach it's maximum point around M equals 1 to 5. With smaller diode sizes, the PCE is major determined by ohmic resistance. So if the junction area increases, the ohmic resistance decrease and the PCE go up. However, when the junction capacitance becomes the determinations, the PCE will goes down with the diode size. From this point of view, we should make the diode ohmic resistance as little as possible while remaining the junction area to be small enough so as to decrease the CJ. There is another issue we have to take into account. With smaller diode sizes, the PCE are higher for light load. However, the trend is vice versa at larger diode sizes. Does it mean our conjecture of the relationship between load and PCE is wrong?

In order to find out the reason why PCE is going down, we plot out the PCE vs. output voltage graph. Since the diode resistor goes down with the diode size, the output voltage is going up. The output voltages of the light load are comparatively higher than the heavy load at the same conditions. We can see that the curves bend at about 0.35Volts. The PCE curve of light load is nearly identical with the heavy load for output voltage smaller than 0.35V. And the PCEs of light load are higher for same output voltage than the heavy load ones for the output voltage larger than the bend point. So we can see that the PCE is actually related to the output voltage (for same input level but different diode sizes. For the same output voltage, the relationship between load and PCE is still working. The reason why there are bends seems related to the junction capacitance of the diodes. The CSM08 model simulations do not show such bends.



The graph below shows the PCE vs. output voltage of CSM08 diode model. The relationship of PCE and output voltage is linear.



As we know, we use ideal voltage source as the simulation input. Since the CSM08 diode model doesn’t include the junction capacitance, the output voltage is determined by the resistor ratio of Rload/(Rload+Rdiode_equivalent). And the current flow through the Rload and Rdiode_equivalent are same for RMS value. So the PCE would be in direct ratio with the output voltage. As for the junction capacitance effect, we will spend more time on it at our second stage research.

(2) NMOS bridge rectifier structure

We can use MOS transistor to form a diode to fulfill a bridge rectifier structure. The figure 3 shows the NMOS bridge rectifier structure configuration.

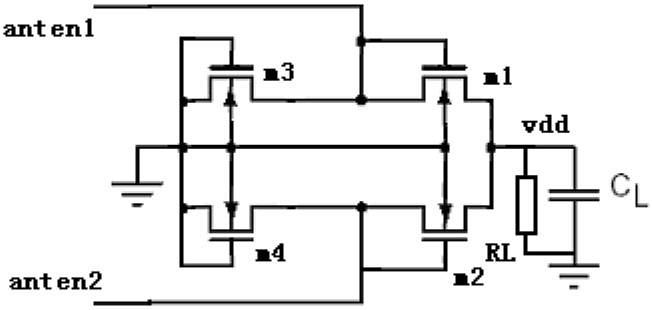
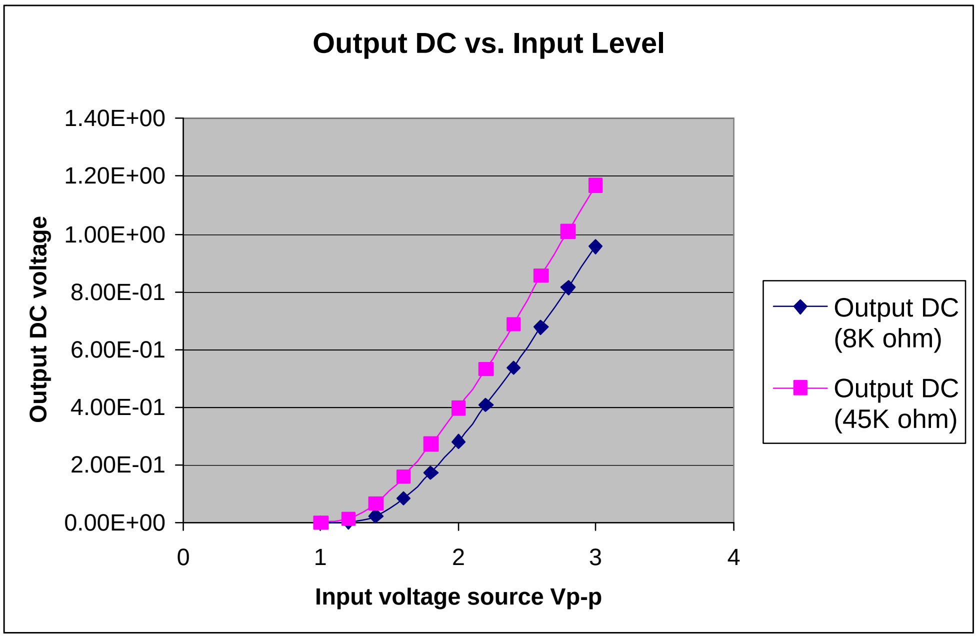


fig. 3

The structure is very common and widely used in the HF contact-less smart card RF interfaces. The substrates of the four MOS diodes are connected to chip ground. The input voltage source is directly added onto the two antenna ports.

(2.1) Minimum working input level

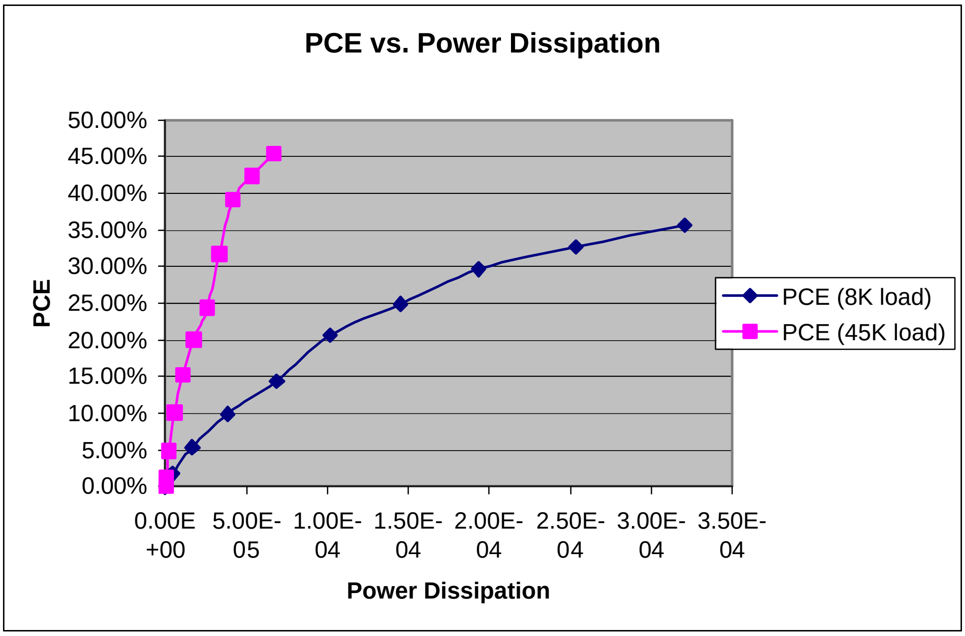
This structure will start to work only when the input level exceeds 2 times of the NMOS turn on voltage, which is around 0.75V for CSM06 low voltage NMOS transistors.



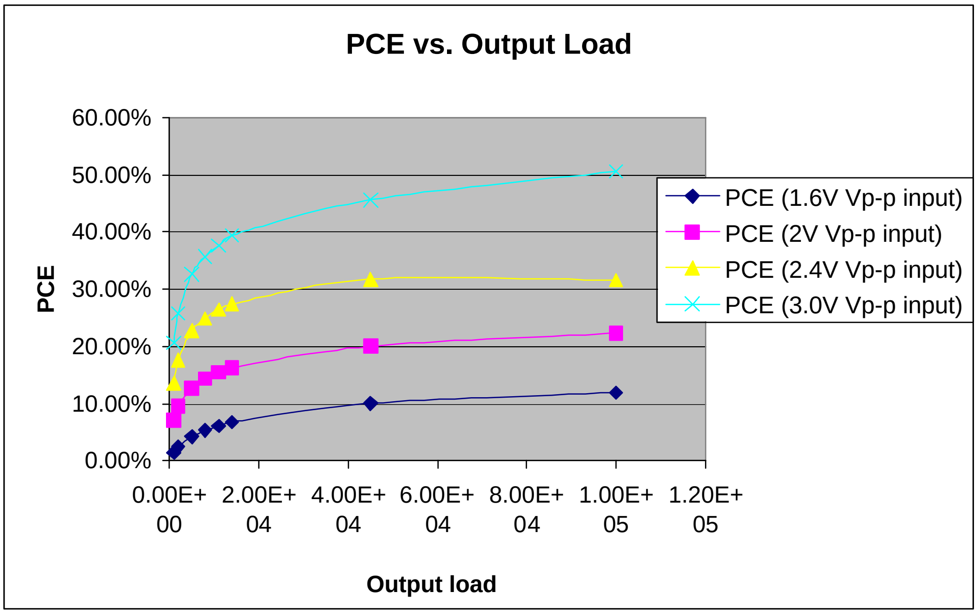
The minimum voltage is around 1.4 volt. However, if the output is considerable, the input voltage level should be more than 2.5 volt.

(2.2) Power Conversion Efficiency (PCE) vs. Input Power

The maximum PCE is near 45% at 3V Vpp input level for 45K ohm load condition. The maximum PCE is over 35% for 8K-ohm load when the power consumption is around 300uW. The power consumption is going up with the input level. We can find out two important clues from the simulation. The first one is that the power conversion efficiency is going down while the load becoming heavier, which is identical with the former two cases. The second one is that the power conversion efficiency is related to the input voltage level as well as the total power consumption. For this structure, the PCE increase cannot compensate the total power consumption increase. That means although we can get higher PCE at higher input voltage level, there is still more absolute power wasted. Or we can say although we can boost up the input voltage level of the rectifier by resonant circuits, the overhead is the power consumption will go high at the same time and results that the optimal PCE still cannot be achieved.



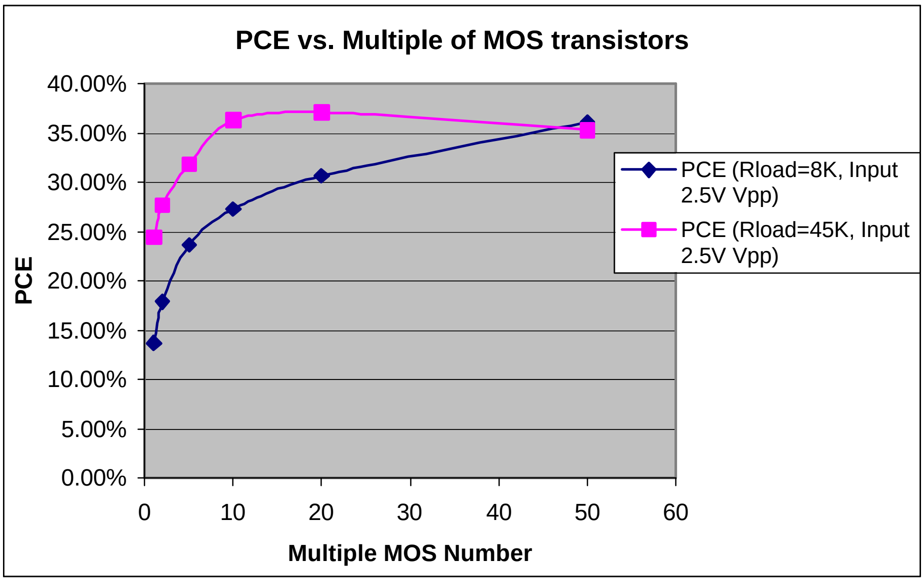
(2.3) Power Conversion Efficiency (PCE) vs. Load

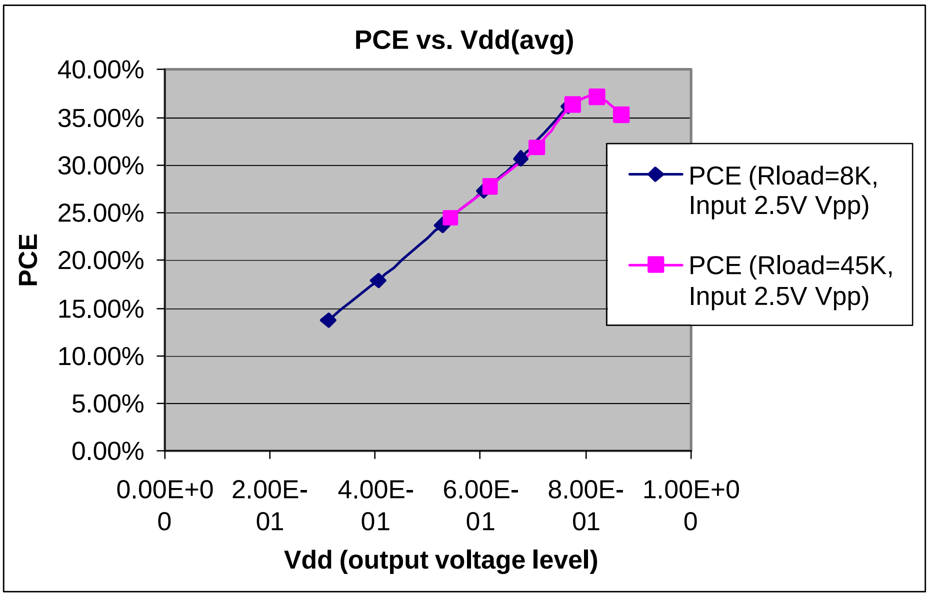


The above chart shows the relationship of PCE and output load. The PCE goes up with the output load resistive value. And the trend becomes flat at higher resistor values. That means even the resistive load is small enough to be omissible, the PCE still cannot be very high. The reason for this is the leakage. A large portion of the work is wasted on the substrate leakage and switching the MOS transistors (channel resistance).

(2.4) Power Conversion Efficiency (PCE) vs. MOS Size (multiple)

The PCE goes high with the multiple of NMOS within a certain size value. For a 45K-ohm load resistor, the PCE has a maximum value at the multiple of 10. And the PCE value of 8K-ohm load resistor goes up all the time according to our simulation conditions. By analyzing the PCE vs. output voltage. We found that the PCE with 45K ohm load has a bend at about 0.8V. And PCE with 8K-ohm load has not reached the output voltage for the given MOS multiple numbers. We will go through this issue again in the phase II research. Besides the leakage caused by capacitance, if we taken the gate ant other nodes resistance into account, we would even not be able to use the rectifier in UHF frequency range if the MOS transistors are too large.





(3) NMOS gate cross-connected bridge rectifier structure

Another common NMOS bridge rectifier structure is shown in figure 4. The two NMOS transistors connected to the chip ground are acting as switches. This configuration can decrease the minimum input working level for an expected output voltage level. However, it does have some drawbacks compared to the normal NMOS diode connected rectifier structures.

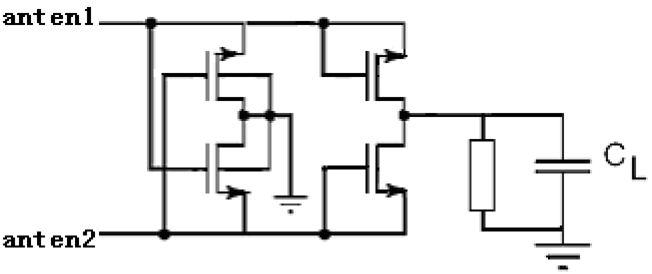
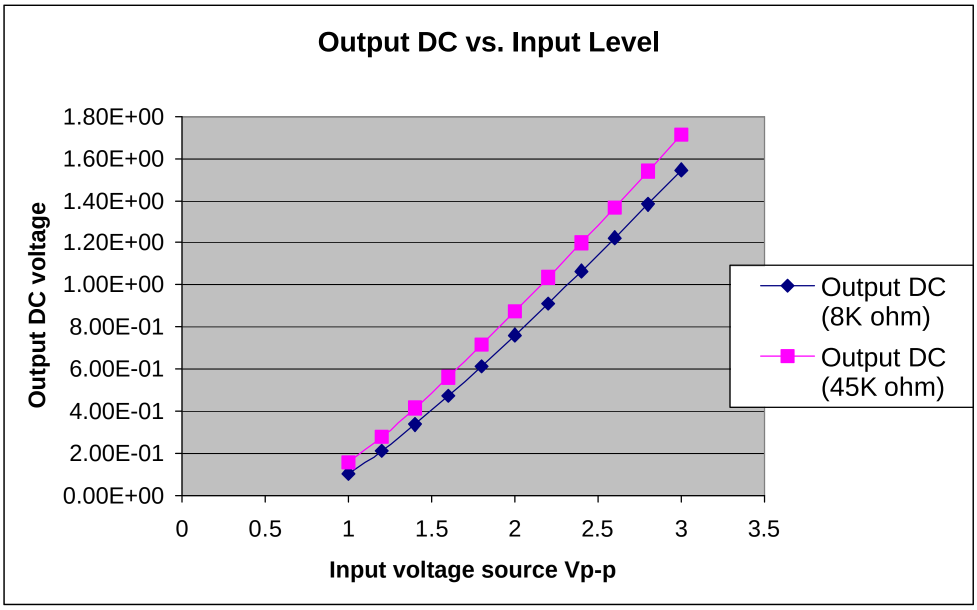


fig. 4

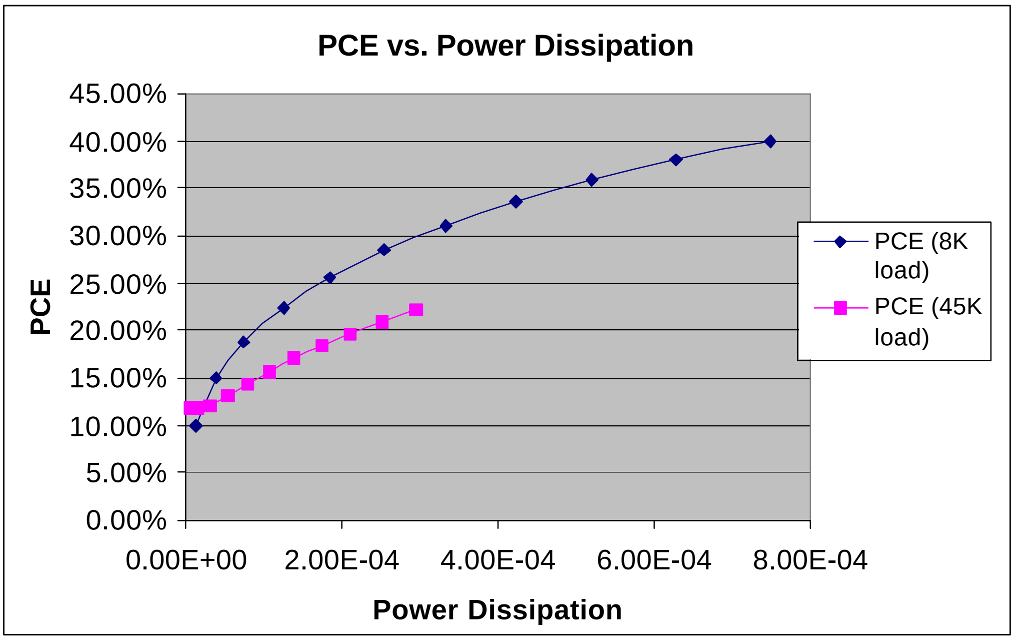
(3.1) Minimum working input level

The minimum working input level is lower than the NMOS diode one as we have mentioned.



(3.2) Power Conversion Efficiency (PCE) vs. Input Power

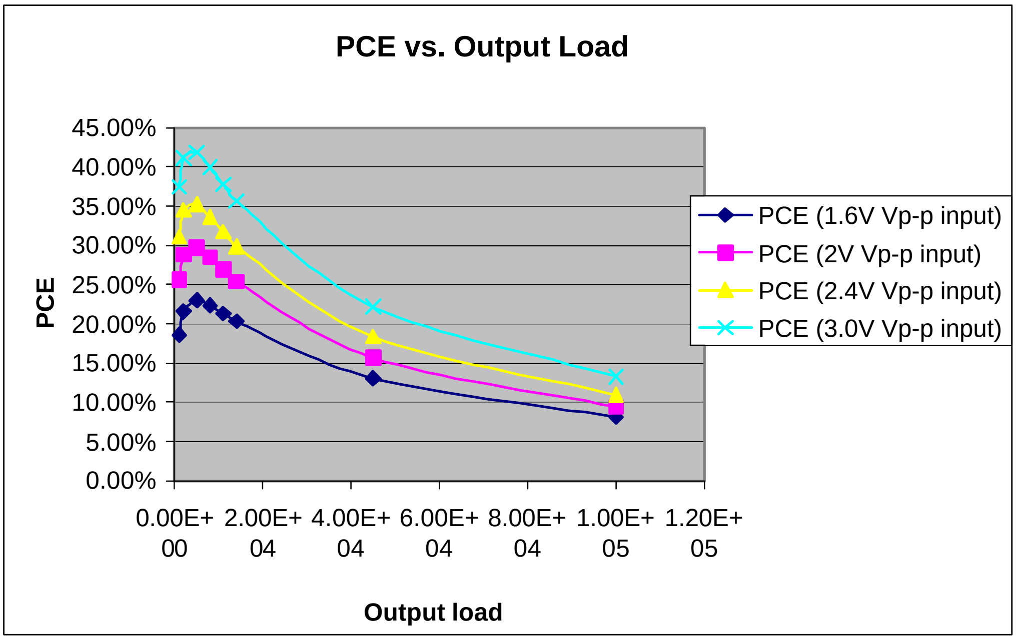
Unlike the former three structures we have analyzed, the PCE of 8K-ohm load is larger than the PCE of 45K ohm load when the input power is greater than 30uW. The reason for this is not very clear by now. We though it shows the capacitive coupling leakage effects of the two gate cross-connected NMOS transistors. And the capacitive coupling leakage portion becomes bigger for smaller load.



At the same time, if we compare the graph with the one of NMOS bridge rectifier, we will find that the PCE of this structure is even lower than the one of NMOS bridge rectifier under same total power dissipation. For example, the PCE of 8K load is around 25% for the power dissipation of 200uW while the PCE of 8K load is around 30% for the case of NMOS bridge rectifier.

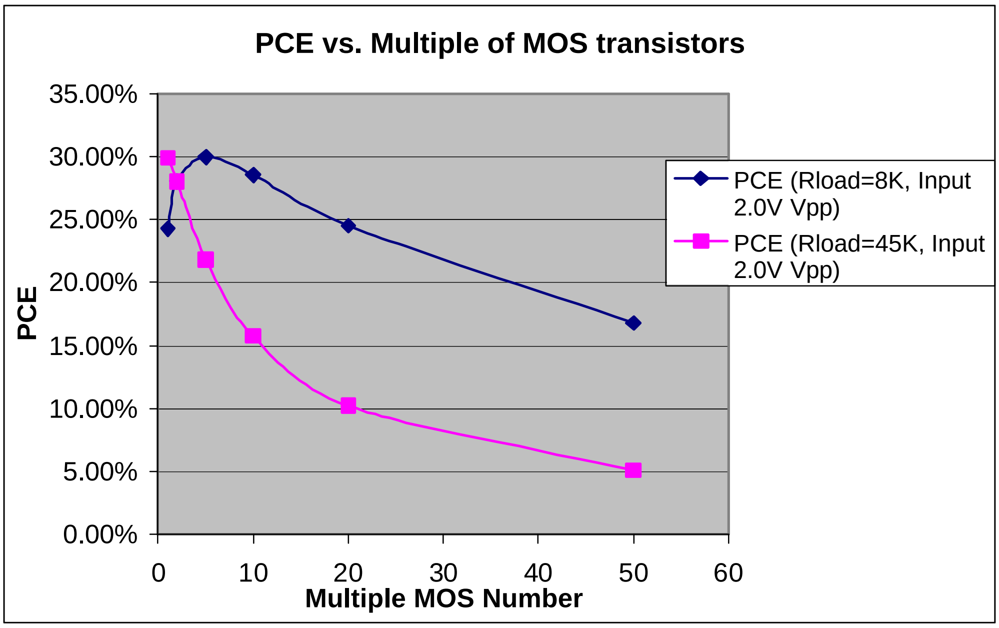
(3.3) Power Conversion Efficiency (PCE) vs. Load

Another interesting phenomenon is considering the PCE and load resistor relationship. Unlike the former three structures, the PCE of the NMOS cross-connected bridge decline sharply with the load resistor value. The maximum values appear at the several kilo-ohms. Just like what we've described in last section, the reason for this is still now clear.



(3.4) Power Conversion Efficiency (PCE) vs. MOS Size (multiple)

The relationship of PCE and MOS size is not surprising with all the simulation works we have already done. The PCE goes down sharply with the increase of the MOS transistor sizes. The capacitance of the MOS transistor is proportional to the size of the MOS transistor. The bigger the size, the bigger the capacitance, and the bigger the capacitance leakage currents. The structure can only maintain reasonable high PCE for the multiple less than 5 of a MOS transistor whose W over L ration is 10u/0.6u. It seems that the structure is not as good as it looks in the UHF frequency range.



(4) PMOS bridge rectifier structure

The counter part of the NMOS bridge rectifier is the PMOS rectifier bridge structures, see figure 5.

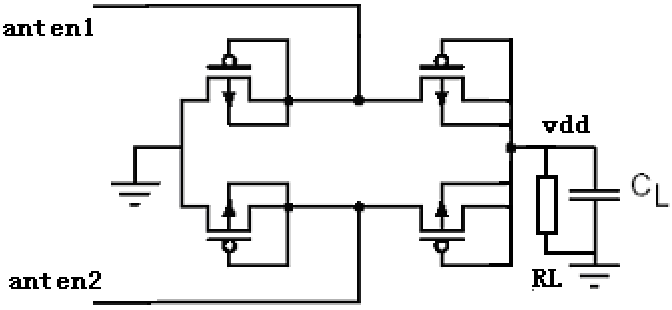
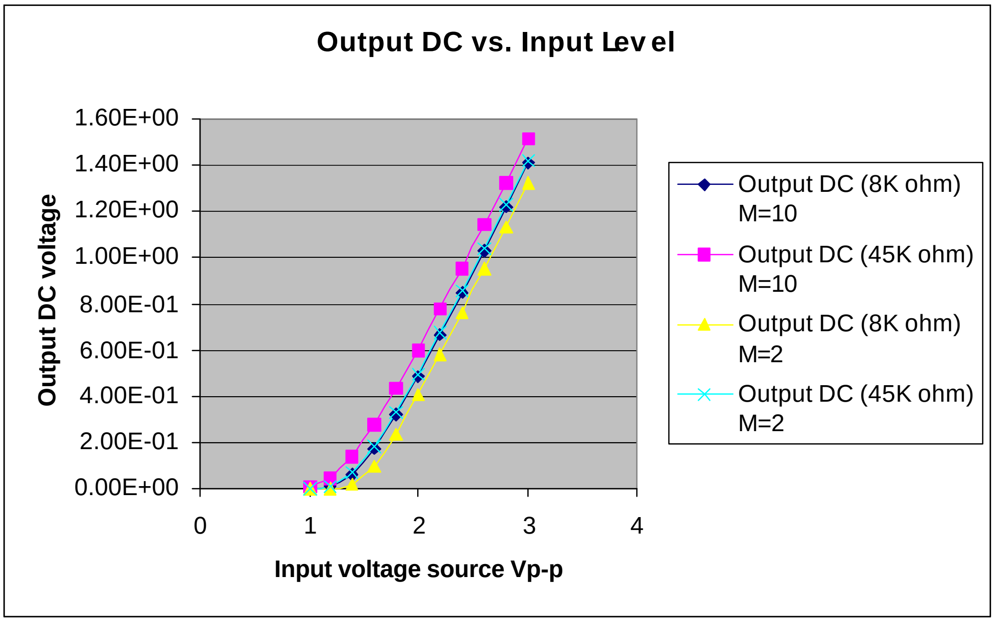


fig. 5

(4.1) Minimum working input level

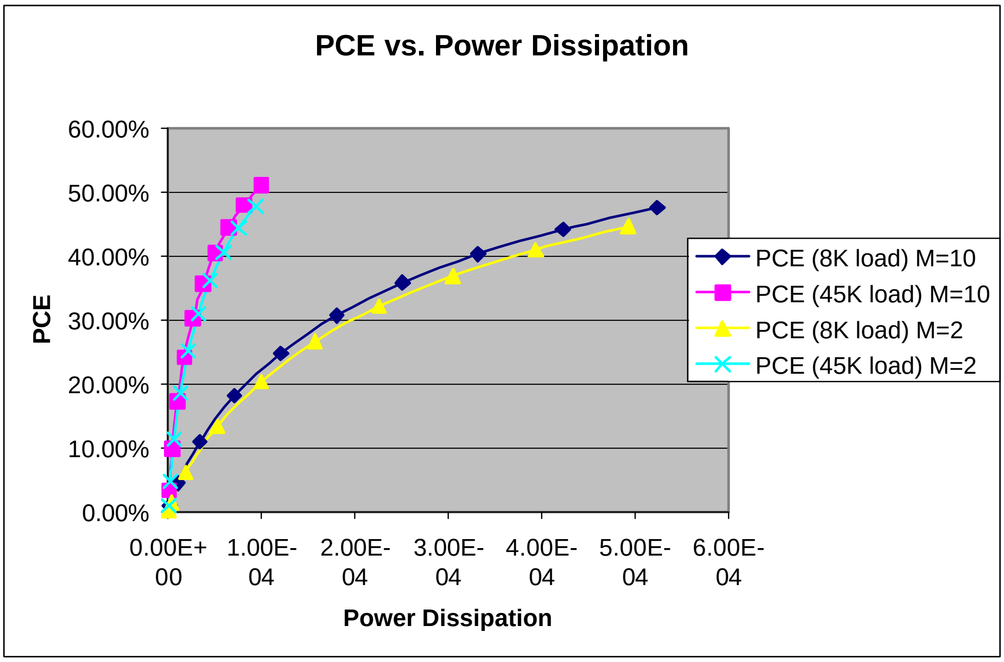
The minimum working input level is closer to the one of NMOS bridge rectifier. The value is around 1.4 to 1.5 volt. However, the output voltage is a little bit higher than its NMOS counter part. The NMOS transistor substrate can only connect to the chip ground and that will increase the turn on voltage of two NMOS transistors that connected between antenna and VDD. The PMOS transistors substrate can be discretely connected and alleviate the effect of substrate bias.

The graph shows four curves. Two are for the multiple of 10. And the other two are for the multiple of 2. We can see that the size of the NMOS transistor will help to increase of the output level.



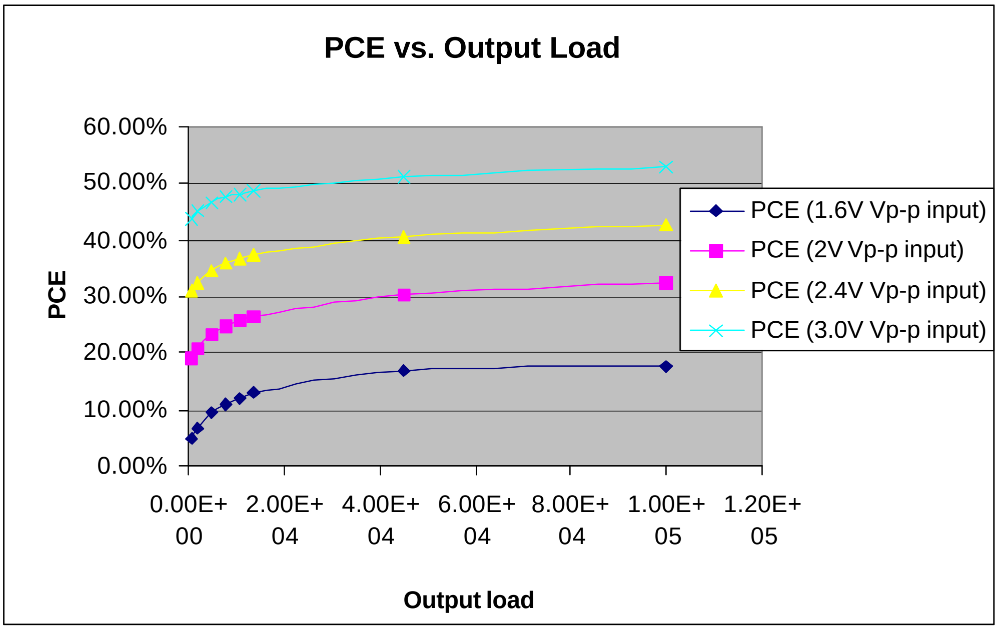
(4.2) Power Conversion Efficiency (PCE) vs. Input Power

The basic trend has come back to this kind of rectifier structure. The lighter the load, the higher the PCE under same power dissipation. In order to compare the results according to the MOS transistor size, we add two data series in. We can see that the PCEs are a little bit higher for multiple of 10 than multiple of 2. However, the power dissipation are higher, too.



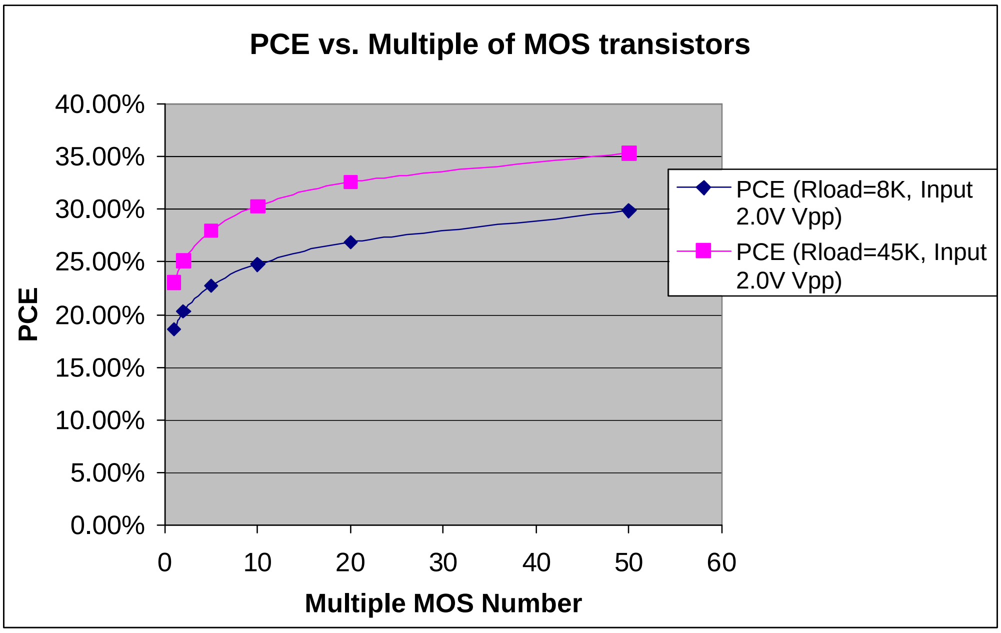
(4.3) Power Conversion Efficiency (PCE) vs. Load

We learned that the multiple of 10 has better PCE than multiple of 2 in last two sections. So we still use multiple of 10 to simulate the relationship between PCE and load. The power conversion efficiency trends show no much difference from the one of NMOS bridge rectifier.



(4.4) Power Conversion Efficiency (PCE) vs. MOS Size (multiple)

The PCE vs. MOS size is the same as the one of CSM08 diode. Or we can say that increase of the MOS size will help the PCE without considering the node resistance.



(5) PMOS gate cross-connected bridge rectifier structure

By cross-connected the gate of two transistors we can form the PMOS gate cross-connected bridge rectifier structure. The structure is showed in figure 6.

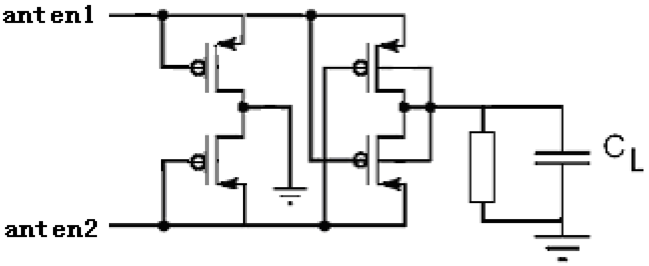
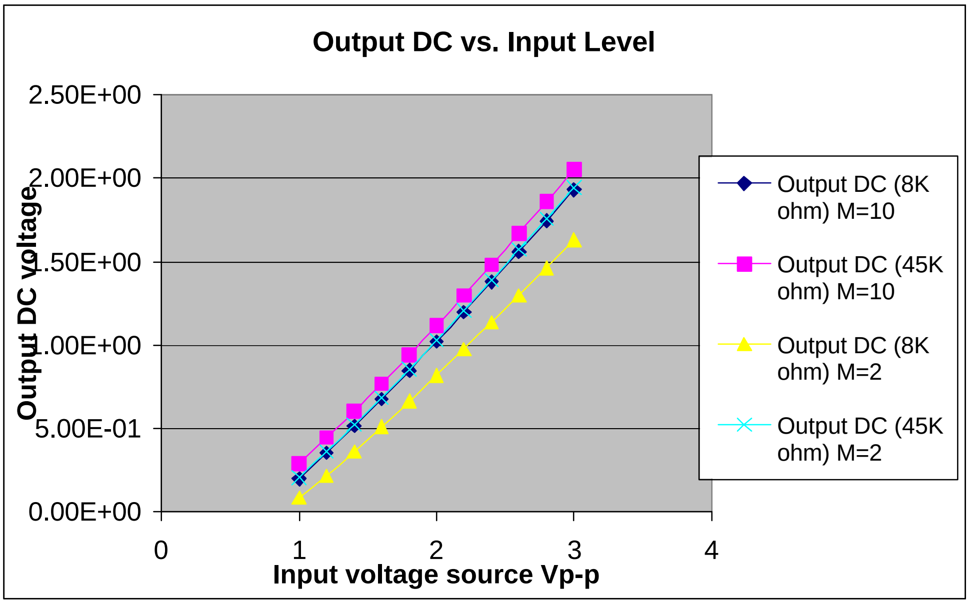


fig. 6

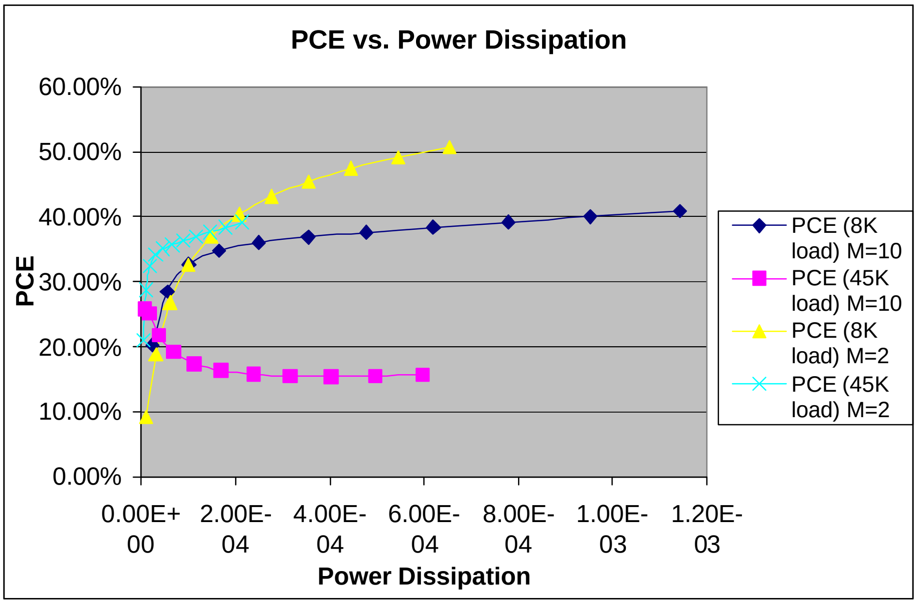
(5.1) Minimum working input level

The minimum working input level is much lower than normal PMOS bridge rectifier. The minimum working input level is below 1 volt. And the curves keep linear relationship with the input level. The graph also shows four curves. Two are for the multiple of 10 and the other two are for the multiple of 2. We can see that the size of the NMOS transistor will help the output level just like what we saw in the PMOS bridge rectifier.



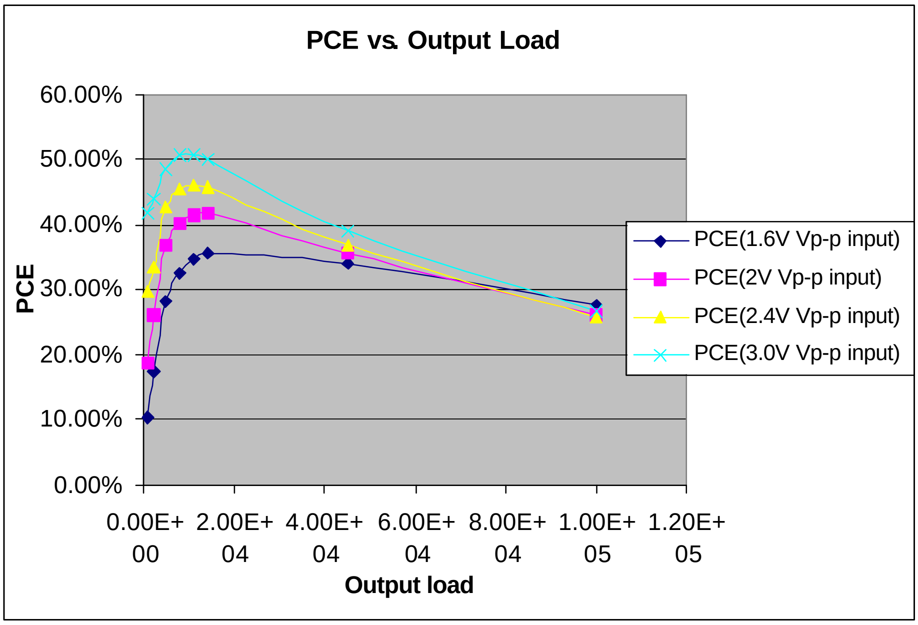
(5.2) Power Conversion Efficiency (PCE) vs. Input Power

The PCE of this structure can reach over 40% with smaller MOS gate size (multiple=2 for the simulation results). The PCE goes up with power dissipation for the case that M equals 2. Since the power dissipation is directlyconnected with the input level. We can see that the parasitic leakage for large transistor size is much more severe than the small one. The total power dissipation is even doubled for large MOS transistors. Another interesting issue is the PCE of M=10 for the load of 45K, the PCE drops with the increase of the input level. This phenomenon is similar to the one of NMOS gate crossconnected rectifier.



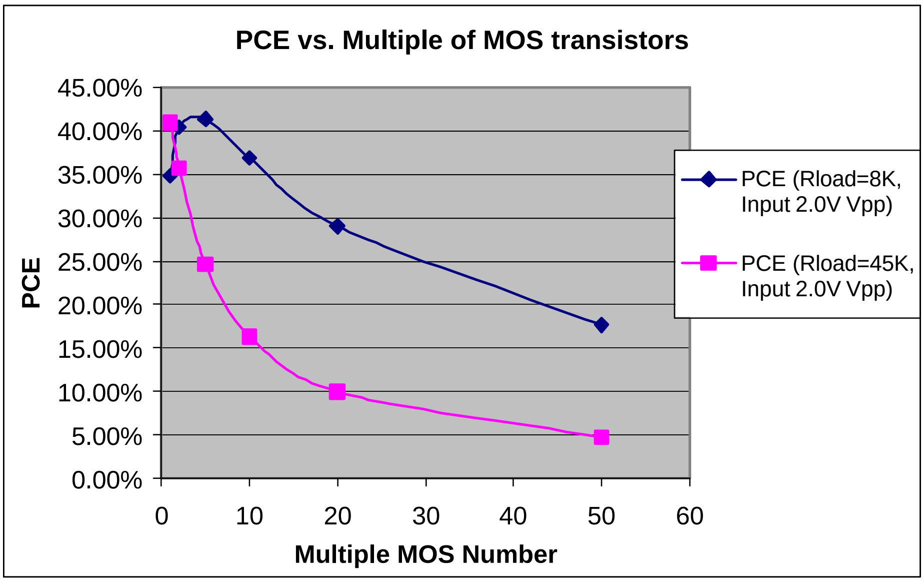
(5.3) Power Conversion Efficiency (PCE) vs. Load

The graph also demonstrates the effect of leakage power consumption. The higher the input level, the more portion will be eaten by leakage (the more sharp decline we can see in the graph).



(5.4) Power Conversion Efficiency (PCE) vs. MOS Size (multiple)

From this graph, we can see the size effects clearly. Although the graph shows less sharp decline for heavier load resistor, we should always remember the absolute waste energy value is much larger for the heavier load. Since the maximum input power is fixed, the case for heavier load is always worse than the lighter one.



(6) PMOS and NMOS gate cross-connected bridge rectifier structure

By combining two cross-connected gate structure, we can get complimentary bridge rectifier structures. The Structure is shown in figure 7. Since we have already researched the effects of transistor size for the past a few structures, we use MOS transistors which size ratio is 10um/0.6um with multiple equals 2 in the simulation of this structure.

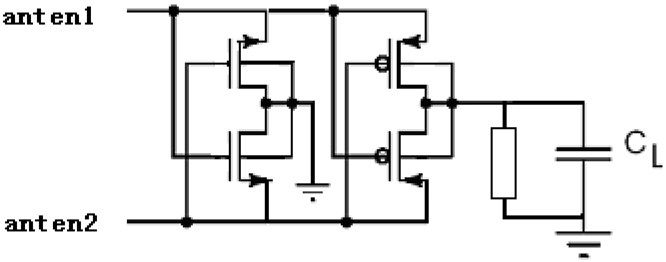
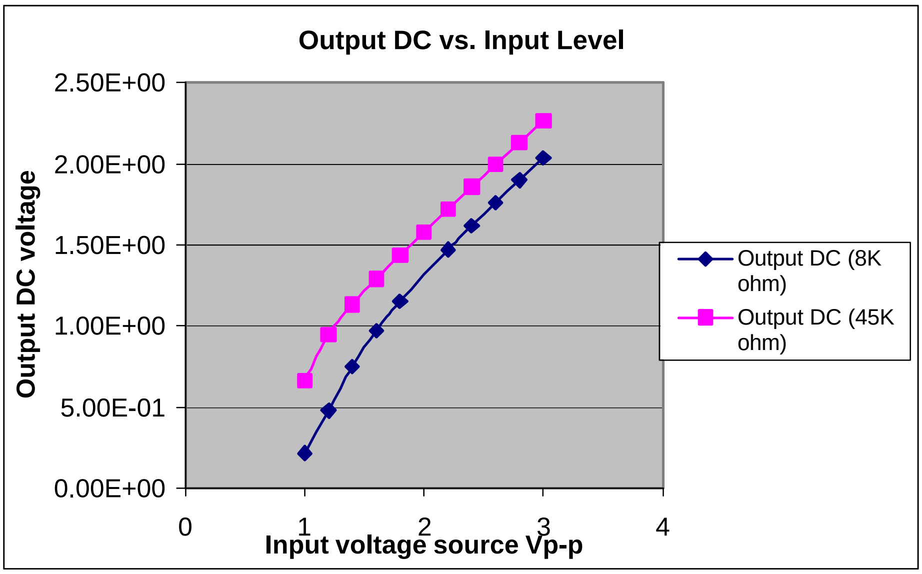


fig. 7

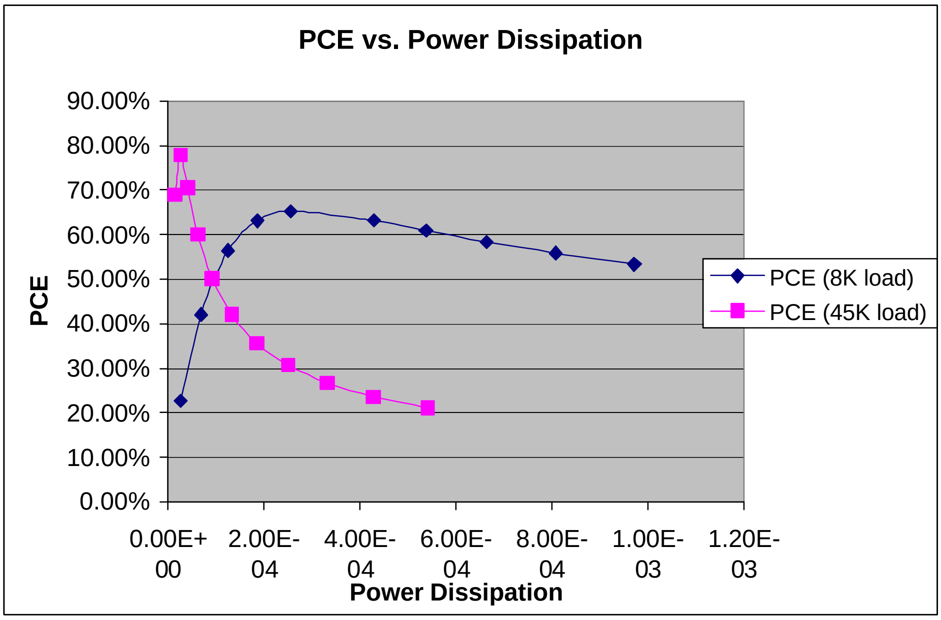
(6.1) Minimum working input level

The minimum working input level is even lower than PMOS gate cross-connected bridge rectifier. The minimum working input level is below 0.5 volt. This is a benefit of changing the working state from MOS diodes to switches. And the output voltage difference between heavy and light load is the most within all the structures we have explored.



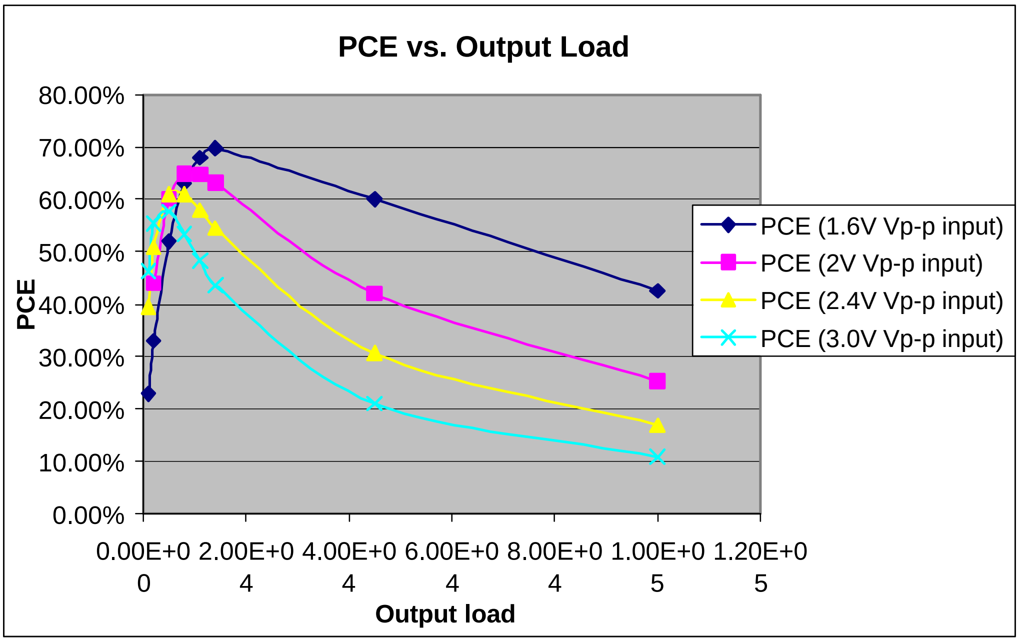
(6.2) Power Conversion Efficiency (PCE) vs. Input Power

The PCE of this structure can reach nearly 80% for light loads. However, if the input voltage level increases, the PCE will drop sharply. This is a heritage of the gate cross-connected structure. There are larger AC voltage drop on the MOS transistor nodes in the gate cross-connected structure. And it will cause more severe leakage than the structures with smaller AC voltage drop on transistor nodes. From this point of view, we can use the structure at low input voltage level. For example, if we want to get a 1.5 Volt output DC value for 45K load, then the input level will be 2.0V. At this input level, the total power dissipation will be around 132uW and the PCE will be 42.08%. If our output DC value is 1.0 Volt, then the total power dissipation will be 186uW for 8K-ohm load and the PCE will reach more than 60%.



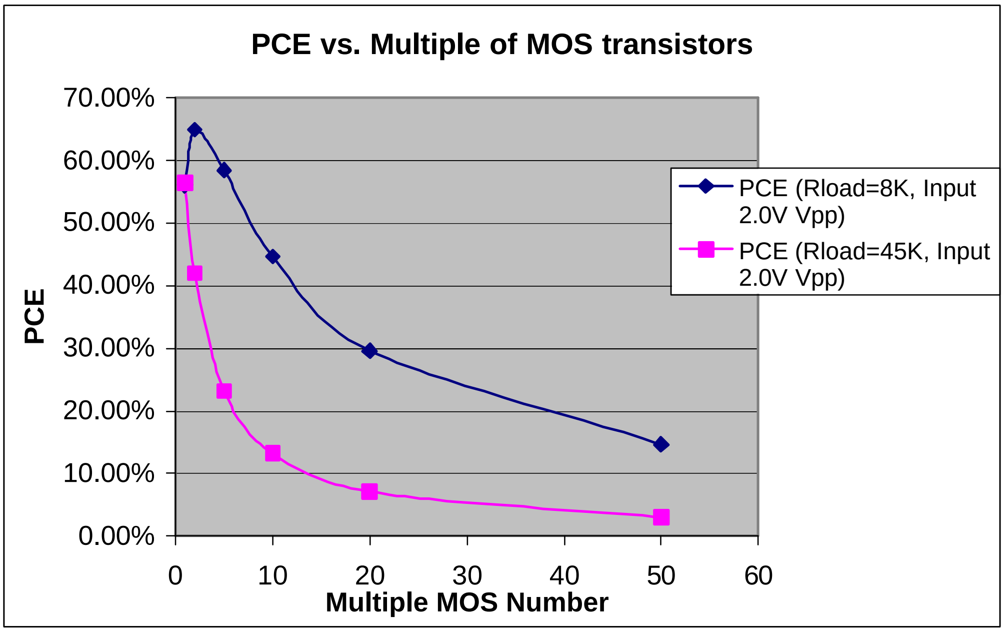
(6.3) Power Conversion Efficiency (PCE) vs. Load

Just like we have analyzed in the previous a few sections. The PCE will goes up first and then go down with the load resistor value. The lower the input voltage level, the higher the peak PCE value. And the PCE will go down with the output load just like any other cross-connected gate structures.



(6.4) Power Conversion Efficiency (PCE) vs. MOS Size (multiple)

There isn't much new information in the simulation except for the relationship between different loads. We can see from the chart that the PCE of light load (45K) is lower than the PCE of heavy load. This is same as the othertwo gate cross-connected structures



(7) 5 stage NMOS diode charge pump rectifier structure

This structure is quite different from the other structures. We can use different stages to get the output voltage level we want. The voltage stage number affects the output voltage, PCE, maximum output power, etc. We just use a 5-stage charge pump as a break point at this time. More research on it will be done in phase II. The structure is shown in figure 8.

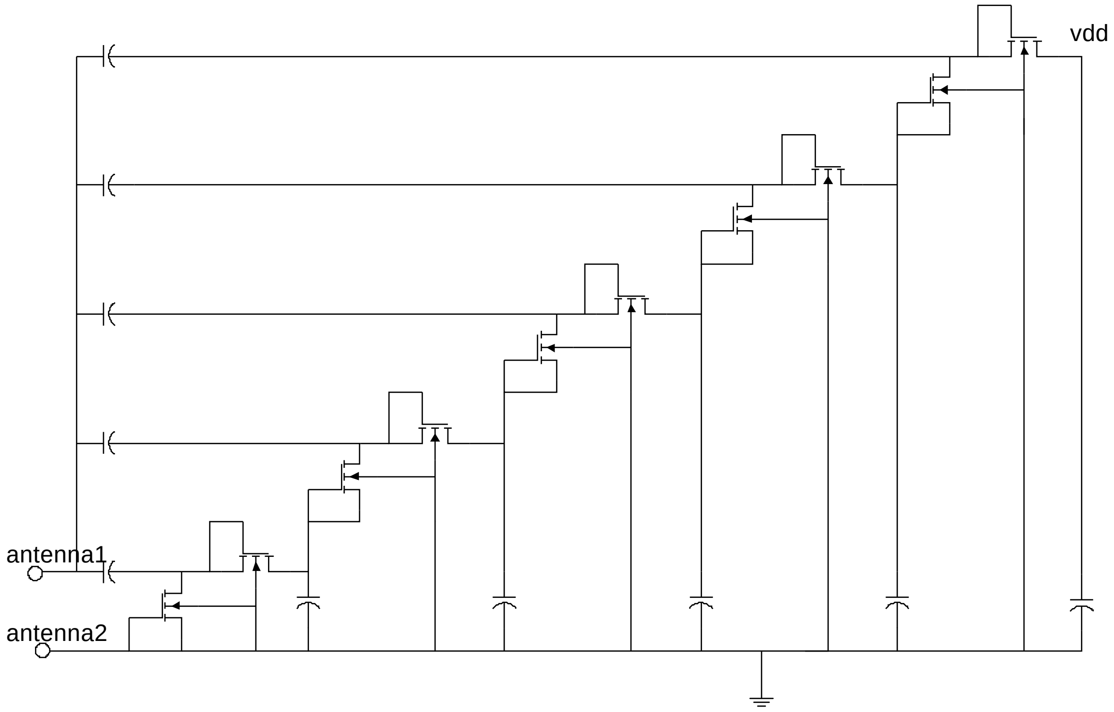
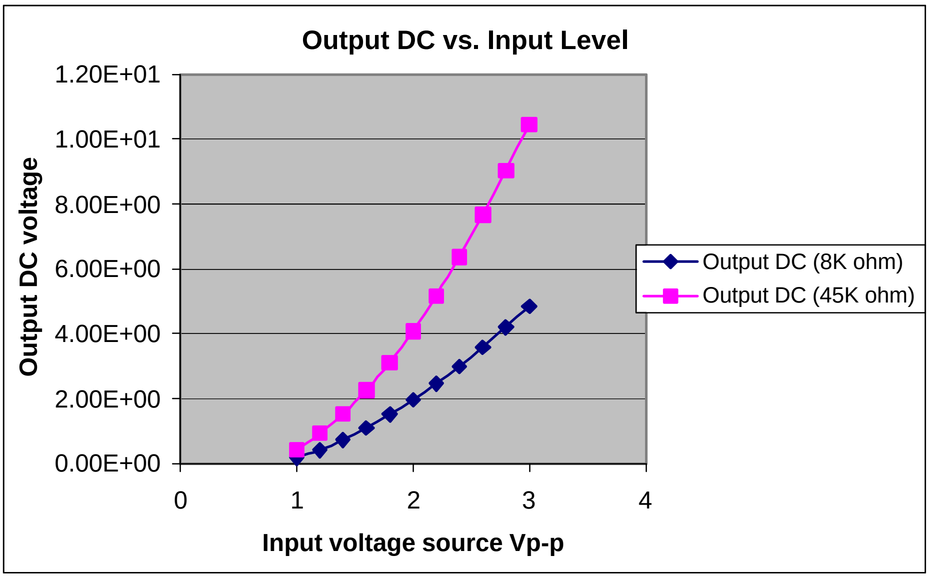


fig. 8

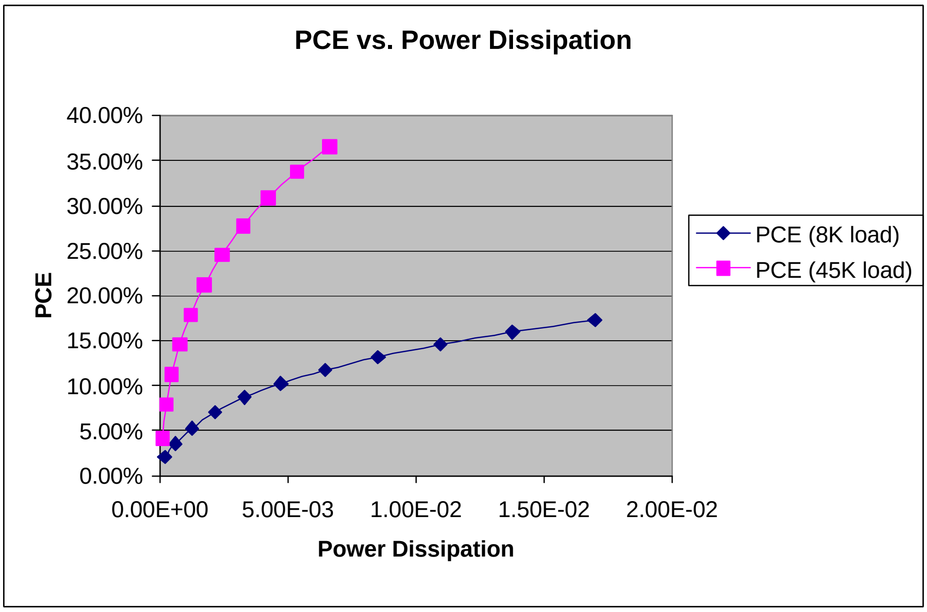
(7.1) Minimum working input level

Since we have to turn on at least one MOS diode, the minimum input level is not as low as the NMOS PMOS complimentary one. The minimum working input level is a little bit lower than 1 volt. However, if we want to get better PCE, the input level should be more than 1.5 Volt.



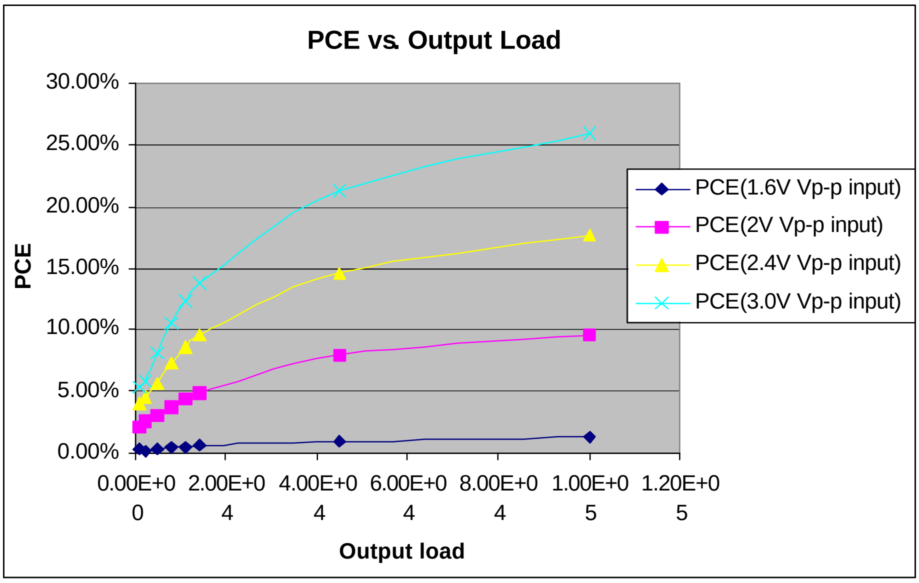
(7.2) Power Conversion Efficiency (PCE) vs. Input Power

The PCE goes high with the power dissipation or the input level. We can see that the power dissipation will be very high if we want to get reasonable high PCE. That means we cannot get higher output voltage and better PCE at the same time. There is a power penalty on the output voltage. Most of the power will be wasted on the pumping process. If we use actual cap model rather than the ideal one which we use for simulation, the results will be even worse because of the leakage. The efficiency of the charge pump is under research for a long period of time.



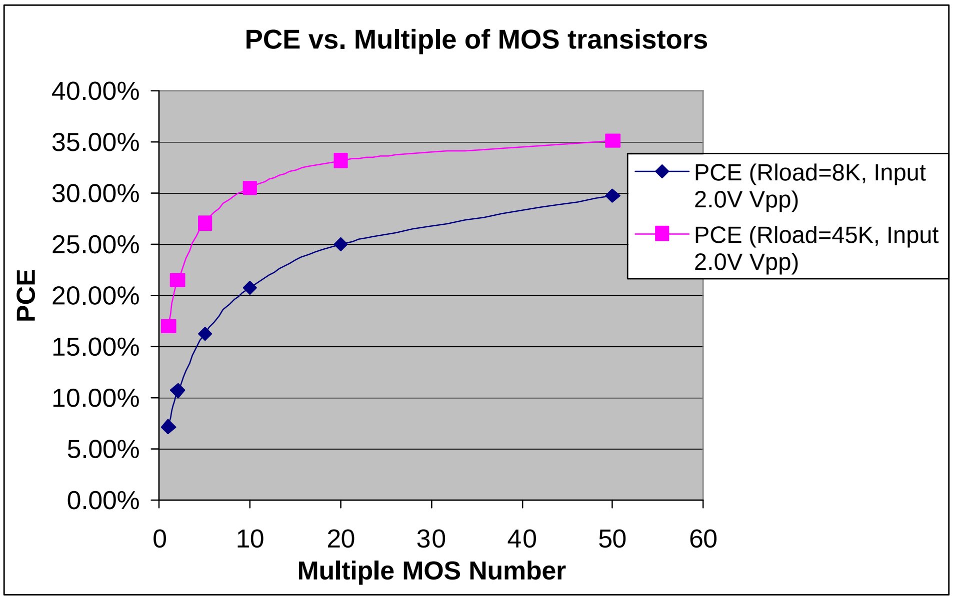
(7.3) Power Conversion Efficiency (PCE) vs. Load

The PCE goes with the output resistive load value. The current consumption of the load is pumped to the VDD node, the more current needed, the more power dissipation wasted in the pump circuits.



(7.4) Power Conversion Efficiency (PCE) vs. MOS Size (multiple)

The PCE will go high with the MOS size. However, if we take a look at the simulation data, we will find that the power dissipation goes high at a faster rate than the PCE does. That means the approach to improve PCE by increase the size of MOS transistors is not working.



Phase I conclusions

After we finished all the simulation work, we are able to make some comparison and analysis on the rectifier structure characteristics. Our comparison is based on two load models. First load case is output working DC voltage equals 1.5Volt and the load power consumption will be 50uW for a 45K-ohm load. The second case is the output working voltage of 2 Volt and the load power consumption is 500uW for a 8K-ohm load.

1.5V, 45Kohm load Minimum input level

	CSM08 diode	CSM06 diode	NMOS brg	NMOS cc brg M=10	PMOS brg M=10	PMOS brg M=2	PMOS cc brg M=10	PMOS cc brg M=2	NMOS PMOS compli	5 stage NMOS chrg pump
Input Level Vp-p	>3V	>3V	>3V	2.8	3	>3	2.4	2.52	1.9	1.4
Total Power dissipation	-	-	-	2.51E-04	9.96E-05		3.16E-04	1.30E-04	1.12E-04	4.66E-04
PCE	-	-	-	21%	51%	-	16%	37.30%	46%	11%

We can see that no rectifier structures can be used to generate a power of 1.5V for 45K ohm load with the total power dissipation (available power from air) less than 90uW. The best power consumption index is achieved by PMOS bridge rectifier (MOS transistor feature size is W/L=10u/0.6u and M=10). However, the input level should be around 3 volt to get the output DC voltage level. If we alleviate the power dissipation control, we will find that the NMOS and PMOS gate cross-connected structure is very attractive. The input level is 1.9 V and the PCE reaches 46% (MOS transistor feature size is W/L=10u/0.6u and M=2). And the lowest input voltage level is achieved by 5 stage NMOS charge pump structure while its power dissipation is the largest of all the rectifier structures.

2V, 8Kohm load Minimum input level

	CSM08 diode	CSM06 diode	NMOS brg	NMOS cc brg M=10	PMOS brg M=10	PMOS brg M=2	PMOS cc brg M=10	PMOS cc brg M=2	NMOS PMOS compli	5 stage NMOS chrg pump
Input Level Vp-p	>3V	>3V	>3V	>3	>3	>3	>3	>3	3	2.0
Total Power dissipation	-	-	-	-	-	-	1.14E-3(at 1.93V)	-	9.71E-04	4.67E-03
PCE	-	-	-	-	-	-	40.8%	-	53.3%	10.7%

The simulation results show the same trend for the 2V, 8K-ohm load condition. The minimum working power would be 971uW. You cannot support such a high power for UHF RFID (The power budget of 500uW is normal only for the HF contact-less smart card or RFID). The solution to it is lower the working voltage as well as the load. The most attractive structure is the NMOS and PMOS complimentary rectifier structure.

In the second phase work will be focused on the reason for the PCE differences and optimization of the existing structures. The optimization will be not only on the circuit elements but also on the structure. For example, if we decrease the turn-on voltage of the NMOS diode as well as the working voltage of the chip by more advanced low voltage low power technology or use Schottky diode, the PCE of the charge pump structure will go up according to our simulation work. Another important issue is to decrease the total power consumption of the chip. From the paper[ii], we learned that the total current consumption of the chip should be less than 1.5uA at 1.5V power supply to get a working distance of 9.25m at 4W EIRP (the PCE of that design is around 18%).

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[i] Soumyajit Mandal "Design of power efficient RF-ID tags" (6.375 Class Project Report, MIT)

[ii] Udo Karthaus, and Martin Fischer "Fully Integrated Passive UHF RFID Transponder IC with 16.7uW Minimum RF Input Power" (IEEE Journal of Solid-State Circuits, Vol.38, No. 10, October 2003)